Scalable Optical Coupling between Polymer Waveguides and a Silicon Photonics Chip

Antonio La Porta, Roger Dangel, Daniel Jubin, Norbert Meier, Folkert Horst, and Bert Jan Offrein

IBM Research - Zurich
Table of contents

Motivation

Si photonics system-level integration and chip-level assembly

Adiabatic optical coupling

Summary
Table of contents

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Adiabatic optical coupling
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Data Center IP traffic trend

Over 5 years:
- 3-fold increase of the Global Data Center IP Traffic – 25% compound annual growth rate (CAGR)
- Majority of traffic (75%) remains within the data center

Consequently, increase on:
- Interconnect bandwidth
- Power consumption

Source: Cisco Global Cloud Index, 2014–2019
High-Level Server Architecture

加速器：PCIe，SMP-总线或网络连接
最高增长潜力
光学技术将主导
→ 标准

 courtesy by Dr. Martin Schmatz
Photonics integration roadmap

2008
- Electrical system, optical fibers at card edge only
- IBM Roadrunner

2011
- Optical fibers across the boards
- IBM Power775

Fibers
Photonics technologies for system-level integration

1. Chip-level integration: **CMOS silicon photonics**
   - Silicon photonics provides all required building (except laser) blocks on chip-level
     ▪ Modulators
     ▪ Drivers
     ▪ Detectors
     ▪ Amplifiers
     ▪ WDM filters
     + CMOS electronics

2. System-level integration: **Optical printed circuit board technology**
   - Provide electrical and optical signal routing capability
   - Avoid fiber cable handling at board or carrier level
   - Enable a simultaneous interfacing of electrical and optical connections
   - One step mating of numerous optical interfaces
Table of contents

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Summary
Chip-level assembly of Si photonics

From Si photonics transceiver subassemblies to chip-level assembly

Today

Research Focus

Chip-level Si Photonics assembly

Molex/Luxtera Blazar QSFP Active Optical Cable
Silicon photonics optical coupling

Basic issue

▪ Large optical modal mismatch between a silicon waveguide and a single-mode fiber

Solution

▪ Mode matching by
  – Diffractive structures, e.g. gratings
  – Mode expansion mechanisms
Table of contents

Motivation
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**Adiabatic optical coupling**
Summary
Adiabatic optical coupling using polymer waveguides

**Principle:**
- Contact between the silicon waveguide taper and the polymer waveguide (PWG), achieved by flip-chip bonding, enables adiabatic optical coupling

- Compatible with established electrical assembly
- Simultaneous E/O interfacing
- Scalable to many optical channels

Design of the adiabatic optical coupler

Design details:
- Si width tapered from 100 nm to 350 nm
- 3-linear-segments taper, smoothest taper slope from 140 nm to 300 nm Si width
Single-mode polymer waveguide technology

- **Chip-size**: Single-mode (SM) PWGs on chips (e.g. Si-Ph chips)
- **Wafer-size**: SM PWGs on wafer-size flexible substrates
- **Panel-size**: SM PWGs on panel-size flexible substrates

Standard SM-fiber-matched cross-sections

PWG-to-fiber coupling loss \(\approx 0.5\) dB

Polymer waveguide processing for adiabatic coupling

(1) PWG direct-processing onto Si-photonics chip

(2) Flip-chip bonding approach

Coupler loss characterization scheme

- Light coupled to PWGs by SM optical fiber
- Separation of coupled light to silicon from light remaining in the PWG
- Extraction of optical coupler loss by the optical transmission comparison of the test unit with the reference PWG path
- Variation of total taper length and wavelength sweep

[Image: Test unit]
Coupler loss characterization (1)

Coupler loss measurement:

- Direct-process vs Flip-chip bonding approach
- For \( L_c \geq 1.0 \text{ mm} \):
  - Low coupler loss
  - PDL \( \leq 0.7 \text{ dB} \)

Schematic view of Si-photonics chip with the PWG directly processed on

Schematic view of Si-photonics chip assembled by flip-chip bonding
Alignment tolerance measurement:
- PWG Flip-chip bonded to purposely misaligned Si waveguides on the chip
- Additional 1 dB loss for ±2 μm misalignment
Insertion loss characterization (1)

Insertion loss measurement:

- Wavelength sweep over O-band
  - Full path vs ref. PWG path
- Wavelength dependency mainly in the PWG

Schematic view of Si-photonics chip assembled by flip-chip bonding
Insertion loss characterization (2)

**Insertion loss** statistics:
- High optical channel count
- For $L_C = 1.0$ mm, 1.5 mm, …, 3.0 mm
Insertion loss characterization (3)

Insertion loss measurement:

- Wavelength sweep over C-band
  - Full path vs ref. PWG path
- High PWG propagation loss

Schematic view of Si-photonics chip assembled by flip-chip bonding
Optical back-reflection characterization

High resolution optical reflectometer measurement (HP 8504B)

- No significant back-reflections from the adiabatic coupler
Table of contents

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Summary
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- Chip-level assembly of Si photonics onto the processor package
  - Offers a path to high bandwidth and low cost optical IO
  - A supply chain ecosystem has to be established

- Adiabatic optical coupling enables efficient, broadband and polarization tolerant chip to polymer waveguide interfacing
  - Compatible with existing electrical assembly processing steps

Path towards high-level of electro-optical integration & scalability
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  - Horizon2020: WIPE and STREAMS

- ..thank you

alp@zurich.ibm.com
Back-up slides

On:

- PDL and wavelength dependent loss
Scattered loss for larger ebeam BSS

Design

e-Beam writing
Scattered light of TE vs TM mode for larger ebeam BSS

TE
$L_C = 1.5 \text{ mm}$
(Offset = 0 $\mu$m)

TM
$L_C = 1.5 \text{ mm}$
(Offset = 0 $\mu$m)