Scalable Optical Coupling between Polymer Waveguides and a Silicon Photonics Chip

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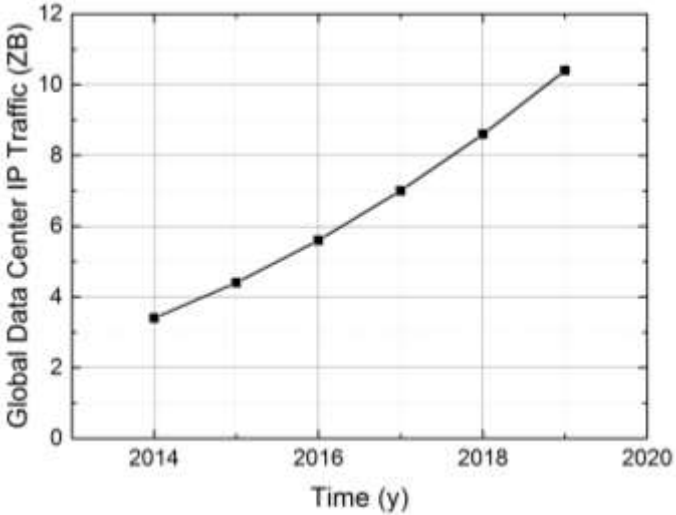
Data Center IP traffic trend



Source: Cisco Global Cloud Index, 2014–2019

Over 5 years:

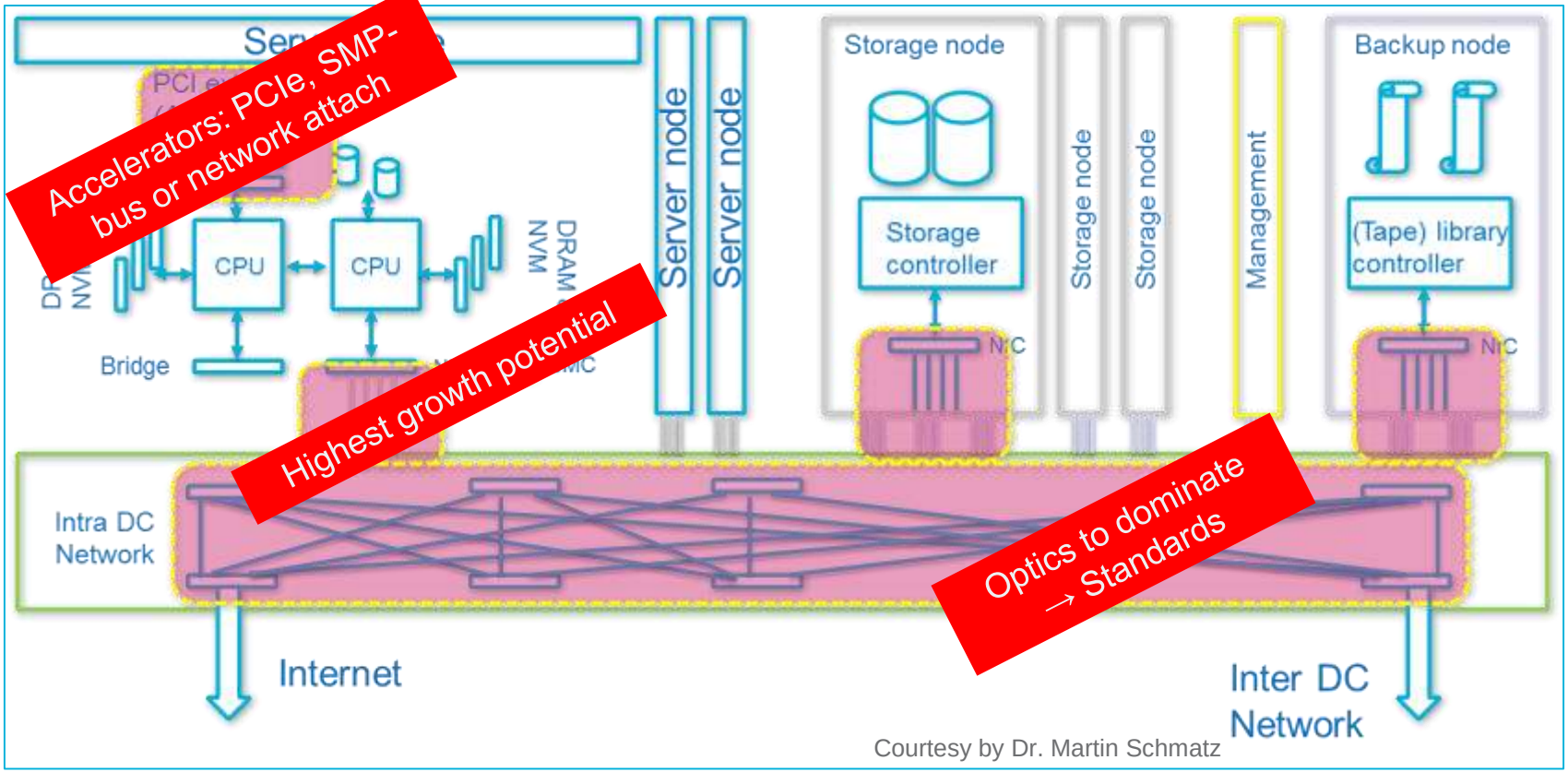
- 3-fold increase of the Globald Data Center IP Traffic
  - 25% compound annual growth rate (CAGR)
- Majority of traffic (75%) remains within the data center

Consequently, increase on:

- Interconnect bandwidth
- Power consumption

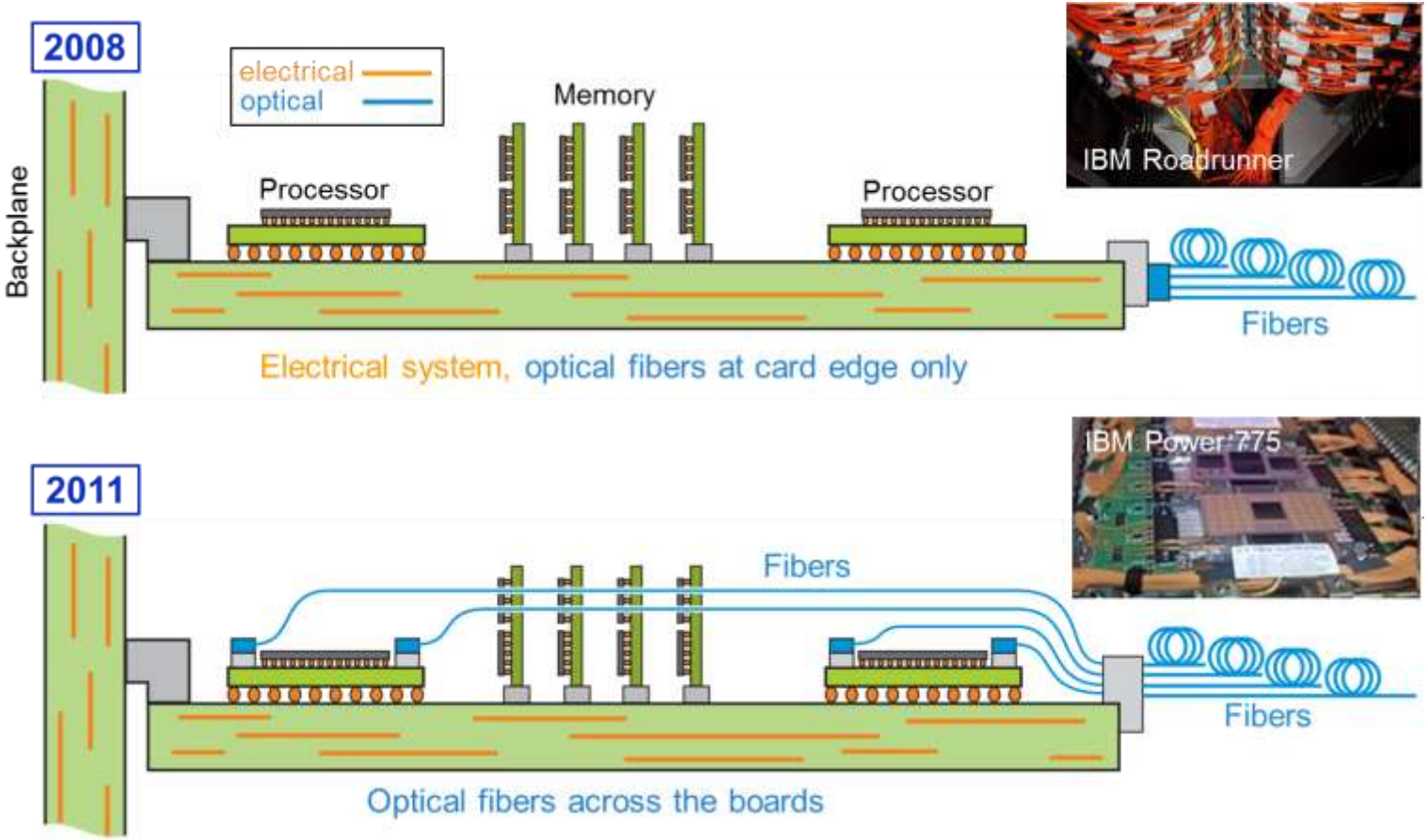
IBM Softlayer Data Center in Sao Paolo, Brasil – Sep. 2015

High-Level Server Architecture



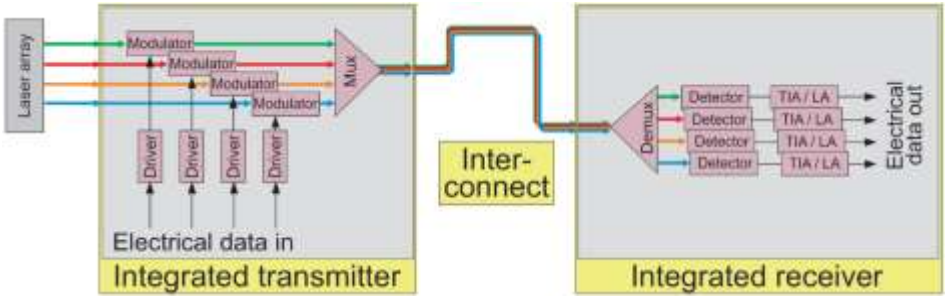
Courtesy by Dr. Martin Schmatz

Photonics integration roadmap



Photonics technologies for system-level integration

1. Chip-level integration: **CMOS silicon photonics**
   – Silicon photonics provides all required building (except laser) blocks on chip-level
      - Modulators
      - Drivers
      - Detectors
      - Amplifiers
      - WDM filters
      + CMOS electronics



2. System-level integration: **Optical printed circuit board technology**
   – Provide electrical and optical signal routing capability
   – Avoid fiber cable handling at board or carrier level
   – Enable a simultaneous interfacing of electrical and optical connections
   – One step mating of numerous optical interfaces

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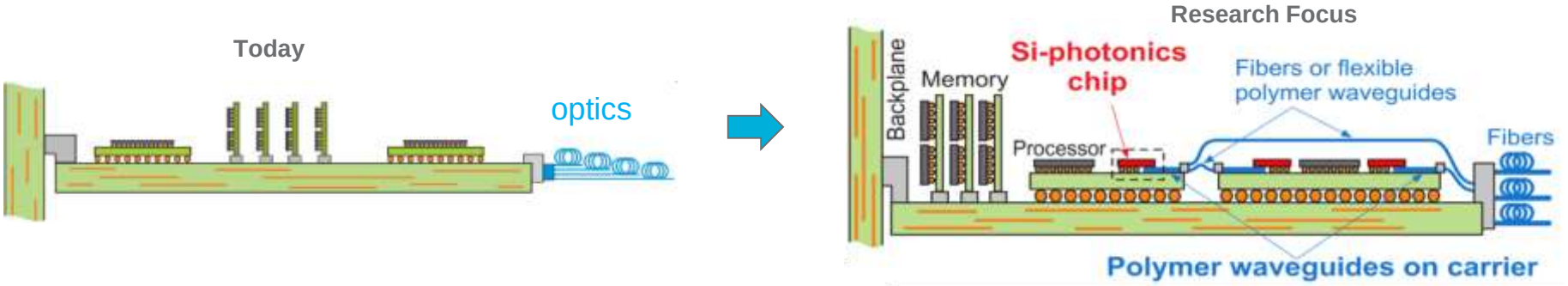
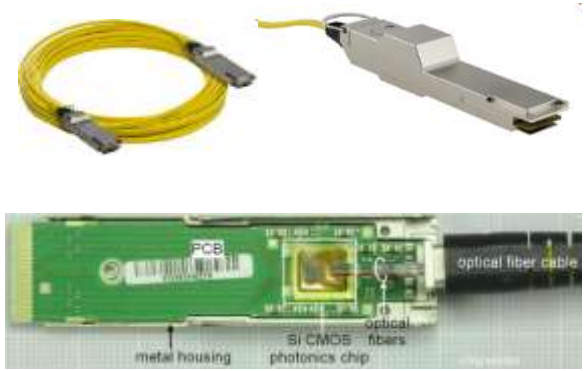
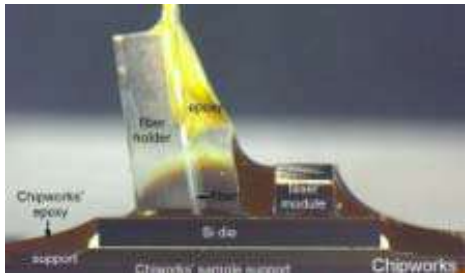
Chip-level assembly of Si photonics

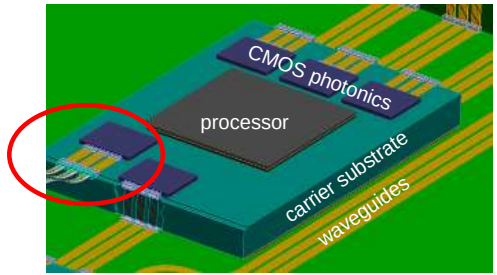
From Si photonics transceiver subassemblies to chip-level assembly





Molex/Luxtera Blazar QSFP Active Optical Cable





Chip-level Si Photonics assembly

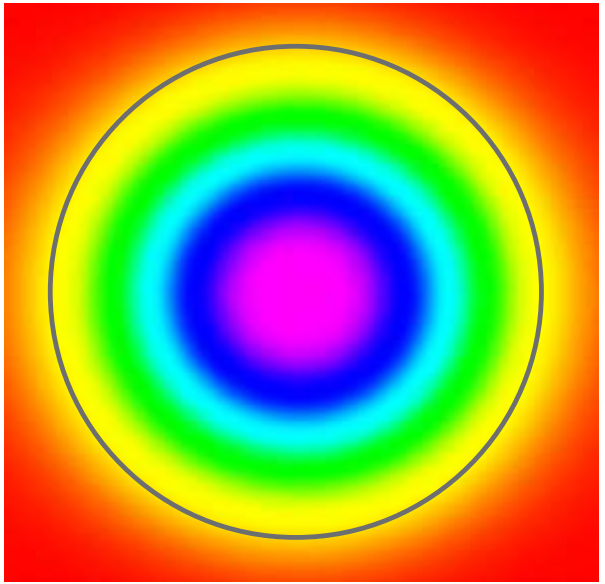
Silicon photonics optical coupling

Basic issue

- Large optical modal mismatch between a silicon waveguide and a single-mode fiber

On-chip silicon waveguide
0.35 x 0.2 µm^2

Single-mode fiber core Ø = 9 µm



Ratio is to-scale

Solution

- Mode matching by
  - Diffractive structures, e.g. gratings
  - Mode expansion mechanisms

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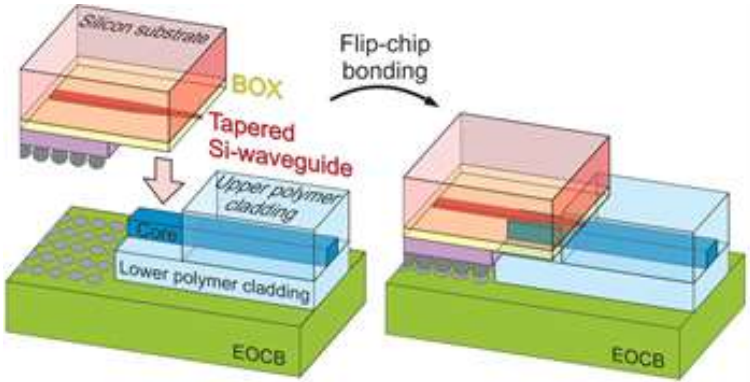
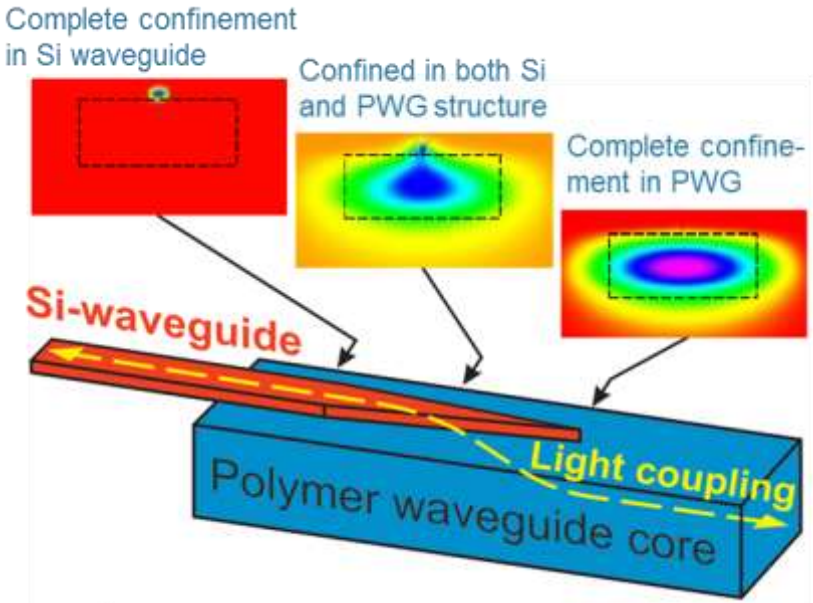
Adiabatic optical coupling using polymer waveguides

Principle:

- Contact between the silicon waveguide taper and the polymer waveguide (PWG), achieved by flip-chip bonding, enables adiabatic optical coupling



Schematic view of Si- photonics chip assembled by flip-chip bonding



- **Compatible with established electrical assembly**
- **Simultaneous E/O interfacing**
- **Scalable to many optical channels**

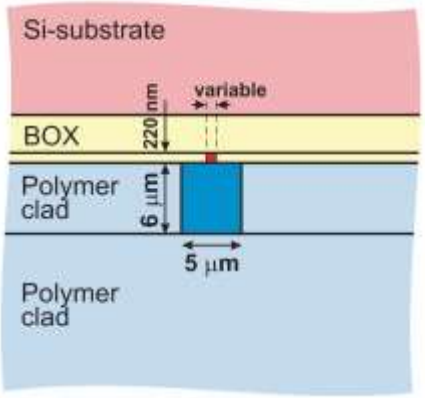
- J. Shu, et al. "Efficient coupler between chip-level and board-level optical waveguides." *Optics letters* 36.18 (2011): 3614-3616.
- I. M. Soganci, et al. "Flip-chip optical couplers with scalable I/O count for silicon photonics." *Optics express* 21.13 (2013): 16075-16085.
- T. Barwicz, et al. "Low-cost interfacing of fibers to nanophotonic waveguides: design for fabrication and assembly tolerances.“, *Photonics Journal, IEEE* 6.4 (2014): 1-18.

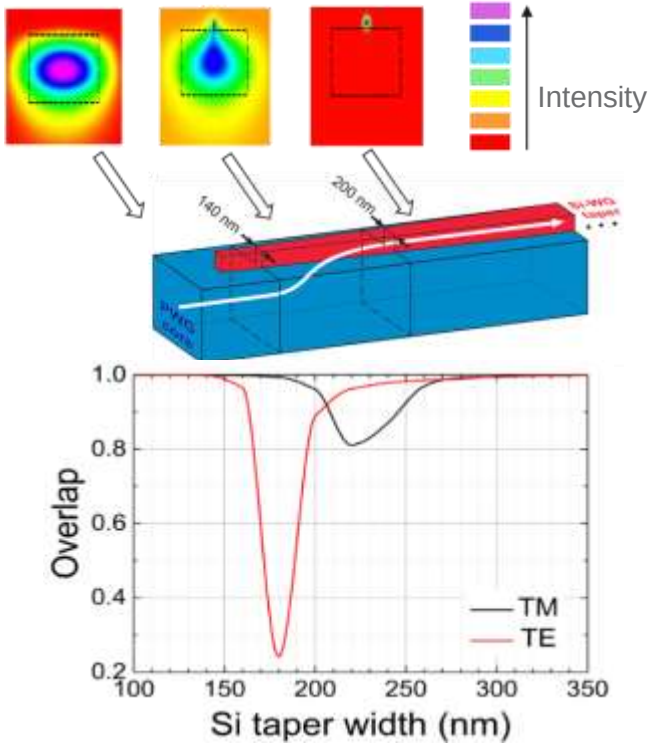
Design of the adiabatic optical coupler

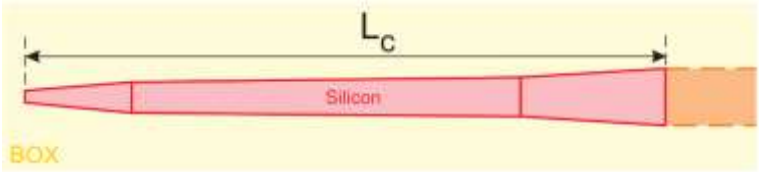
Design details:

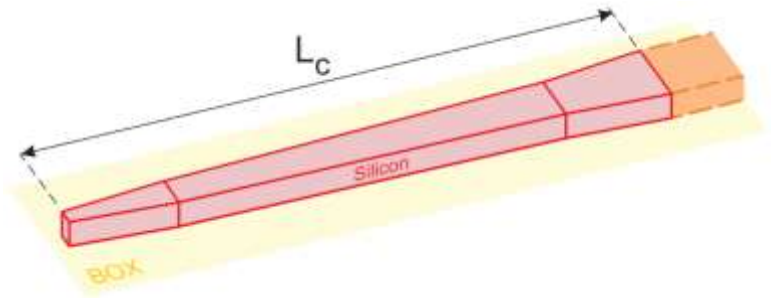
- Si width tapered from 100 nm to 350 nm
- 3-linear-segments taper, smoothest taper slope from 140 nm to 300 nm Si width

Si-WG/PWG system







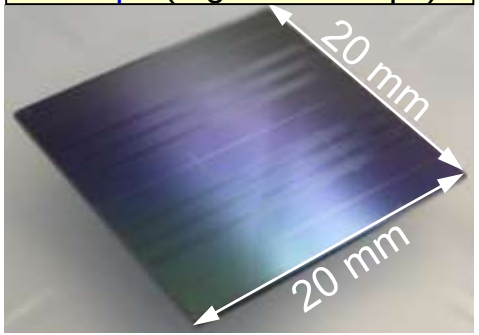


Single-mode polymer waveguide technology

DOW CORNING

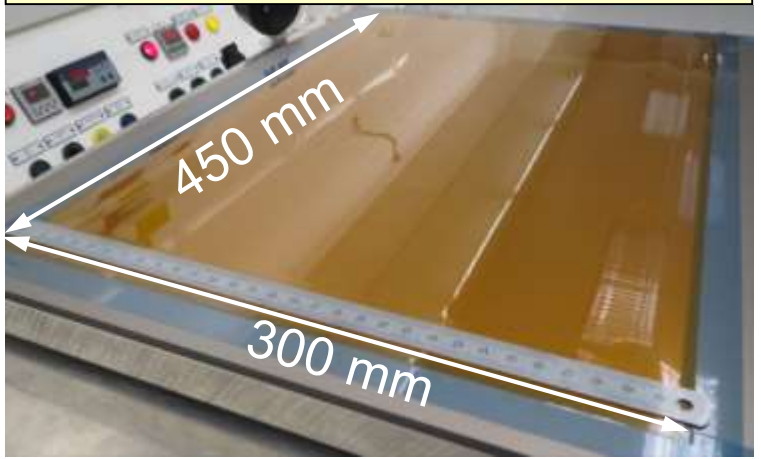
Chip-size

Single-mode (SM) PWGs on chips (e.g. Si-Ph chips)



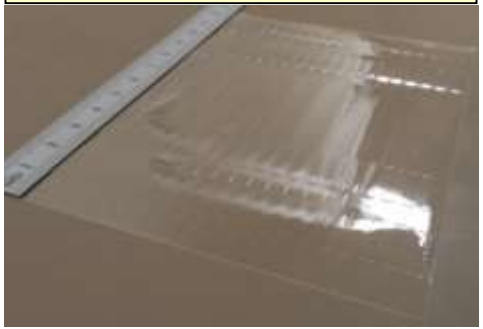
Panel-size

SM PWGs on panel-size flexible substrates



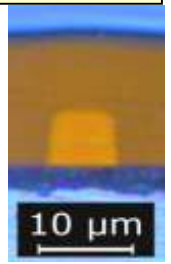
Wafer- size

SM PWGs on wafer-size flexible substrates



Standard SM-fiber-matched cross-sections

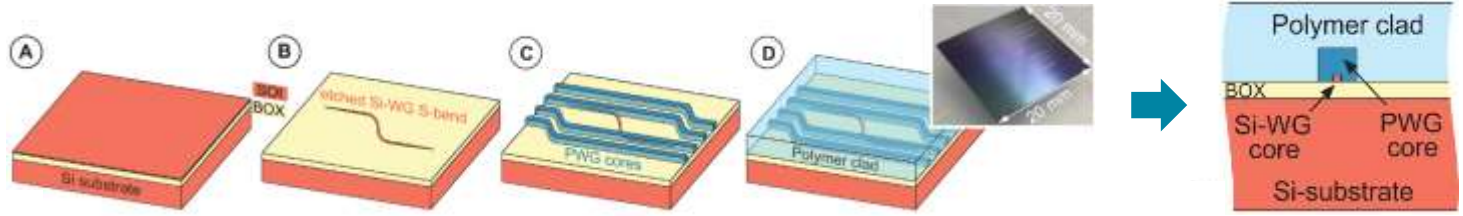
PWG-to-fiber coupling loss ≈ 0.5 dB



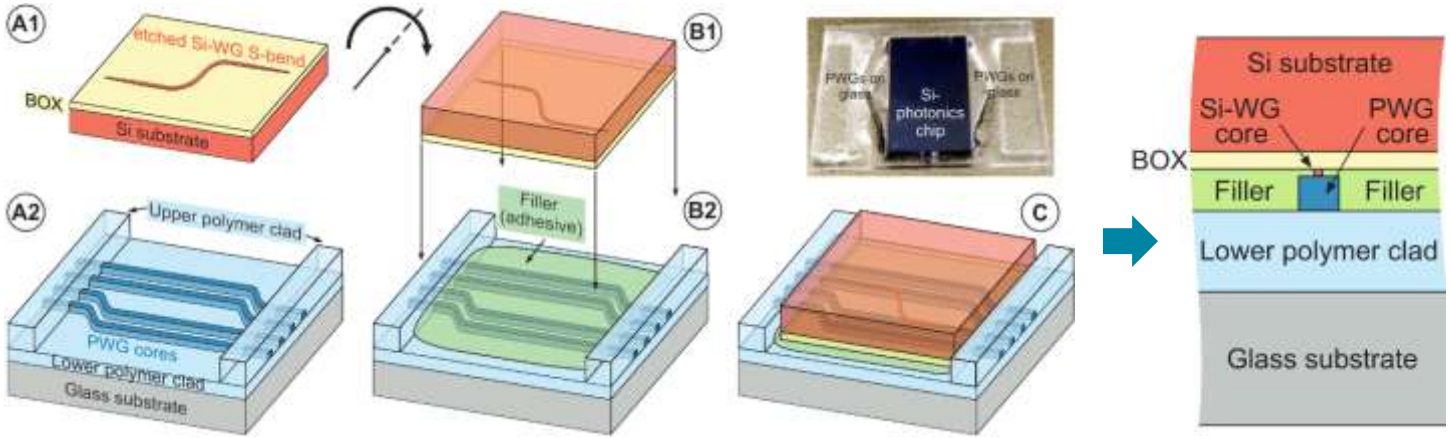
- R. Dangel, et al. "Polymer waveguides for electro-optical integration in data centers and high-performance computers." *Optics express* 23.4 (2015): 4736-4750.

Polymer waveguide processing for adiabatic coupling

(1) PWG direct-processing onto Si-photonics chip



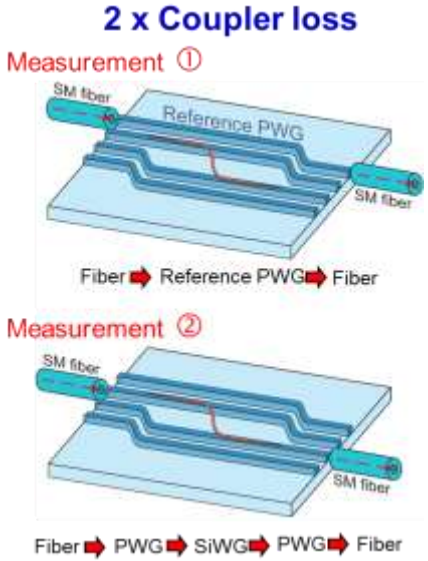
(2) Flip-chip bonding approach

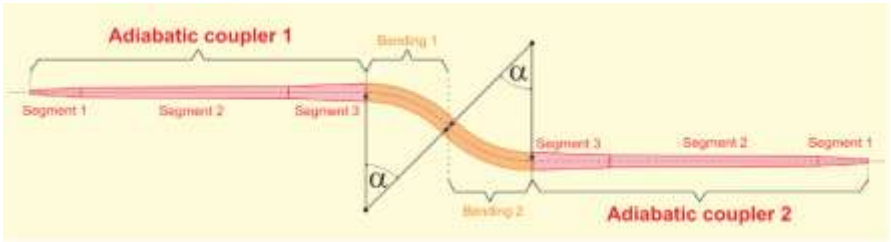


- J. S. McNab, et al. "Ultra-low loss photonic integrated circuit with membrane-type photonic crystal waveguides." *Optics express* 11.22 (2003): 2927-2939.
- A. La Porta, et al. "Silicon photonics packaging for highly scalable optical interconnects." 65th IEEE ECTC, 2015.

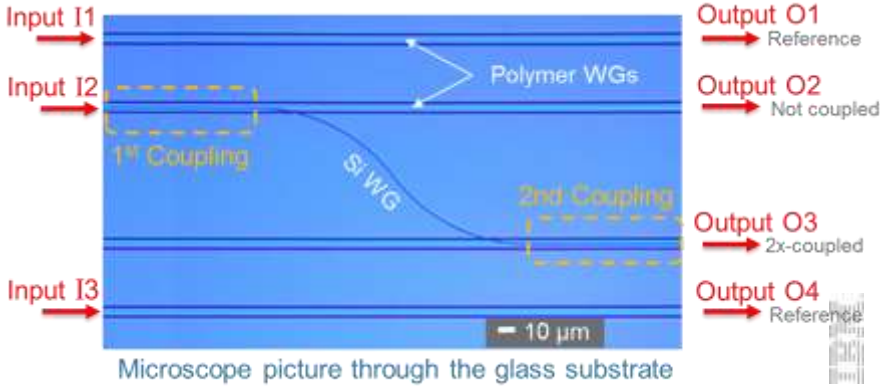
Coupler loss characterization scheme

- Light coupled to PWGs by SM optical fiber
- Separation of coupled light to silicon from light remaining in the PWG
- Extraction of optical coupler loss by the optical transmission comparison of the test unit with the reference PWG path
- Variation of total taper length and wavelength sweep





Test unit

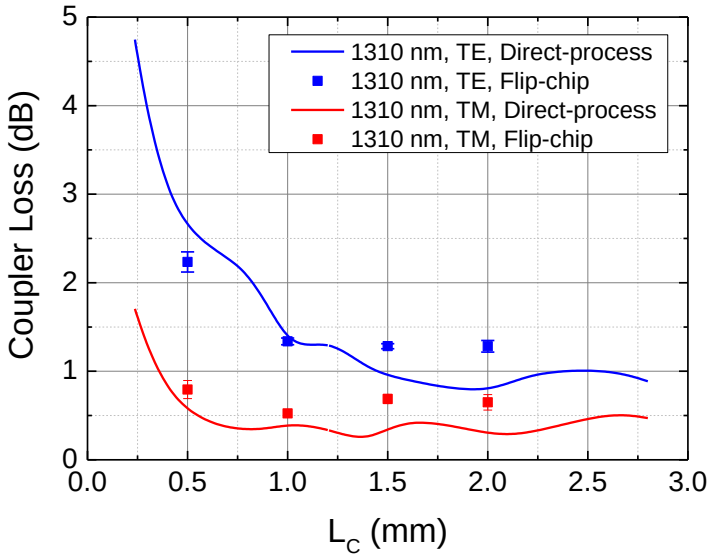


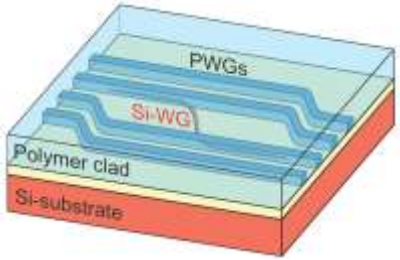
Microscope picture through the glass substrate

Coupler loss characterization (1)

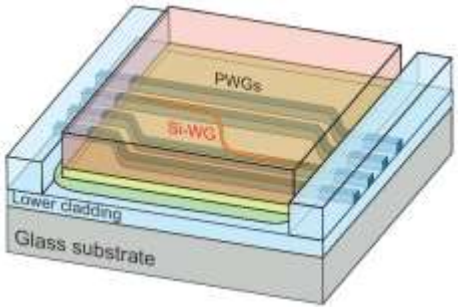
Coupler loss measurement:

- Direct-process vs Flip-chip bonding approach
- For $L_c \geq 1.0$ mm:
  - Low coupler loss
  - PDL ≤ 0.7 dB





Schematic view of Si-photonics chip with the PWG directly processed on

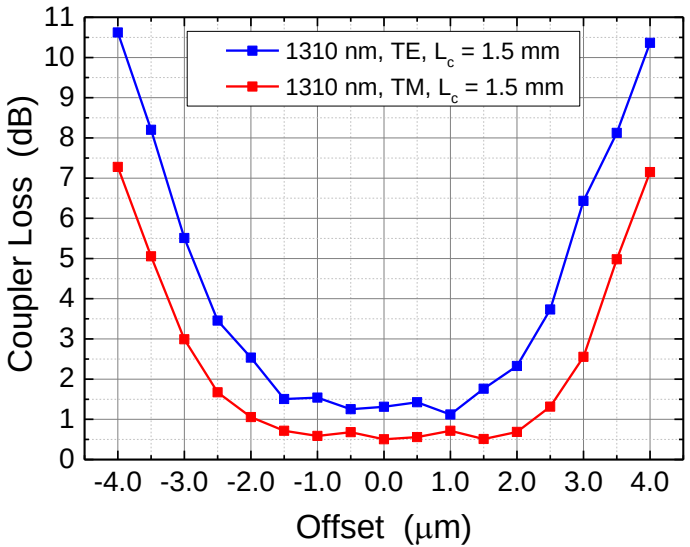


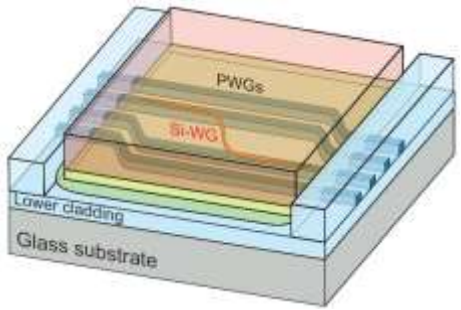
Schematic view of Si-photonics chip assembled by flip-chip bonding

Coupler loss characterization (2)

Alignment tolerance measurement:

- PWG Flip-chip bonded to purposely misaligned Si waveguides on the chip
- Additional 1 dB loss for ±2 μm misalignment



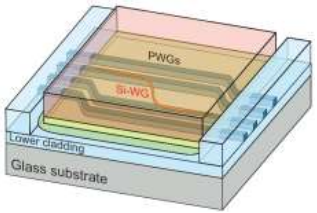


Schematic view of Si-photonics chip assembled by flip-chip bonding

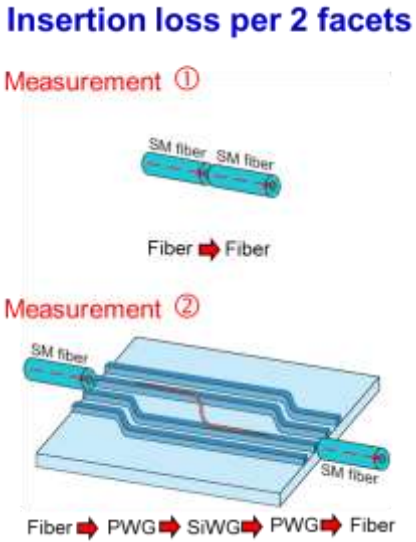
Insertion loss characterization (1)

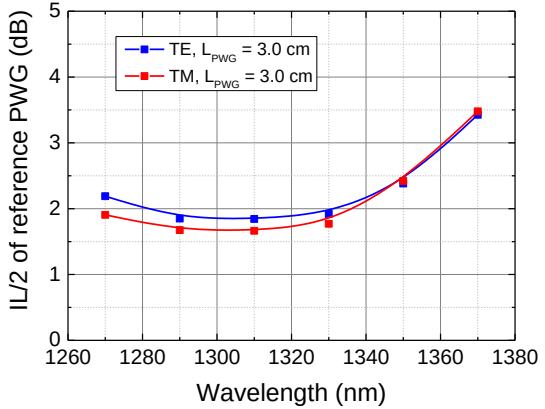
Insertion loss measurement:

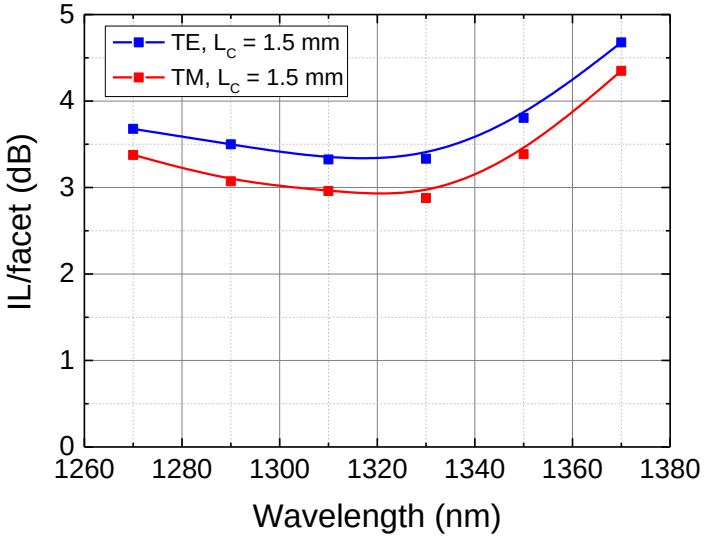
- Wavelength sweep over O-band
  - Full path vs ref. PWG path
- Wavelength dependency mainly in the PWG



Schematic view of Si-photonics chip assembled by flip-chip bonding



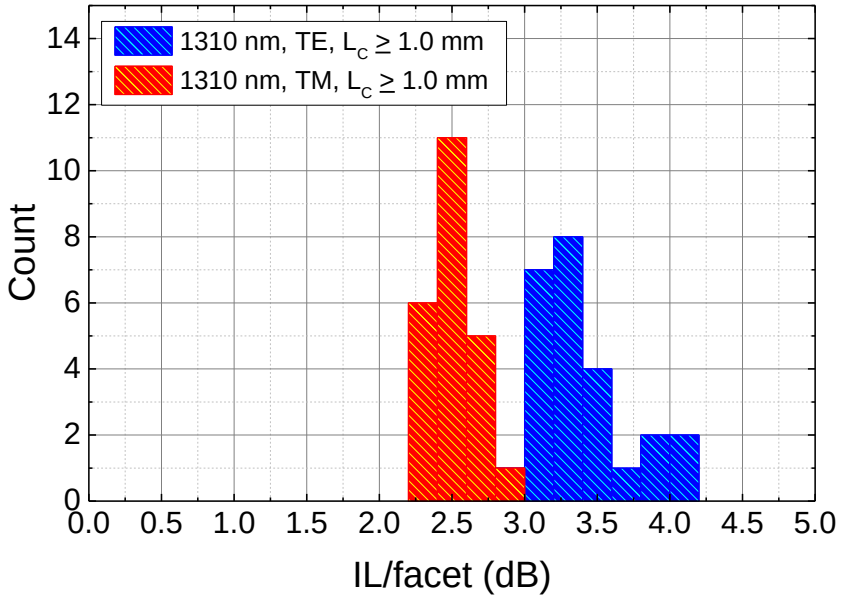


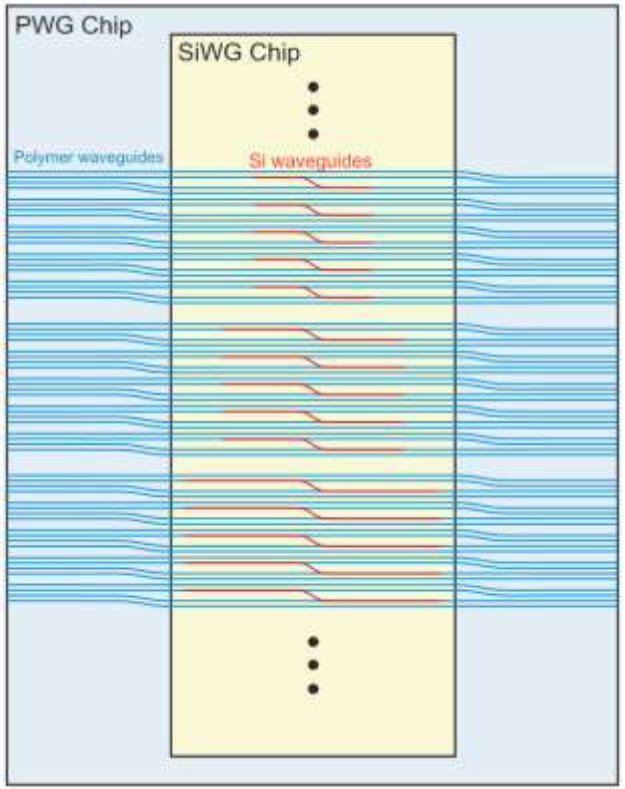


Insertion loss characterization (2)

Insertion loss statistics:

- High optical channel count
- For L_C = 1.0 mm, 1.5 mm, …, 3.0 mm



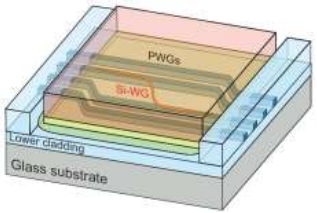


Top-view of Si-photonics chip assembled by flip-chip bonding

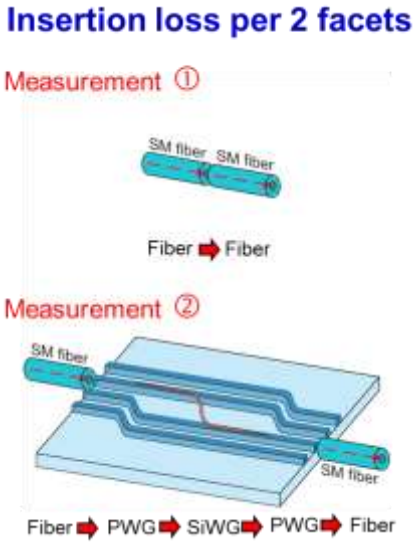
Insertion loss characterization (3)

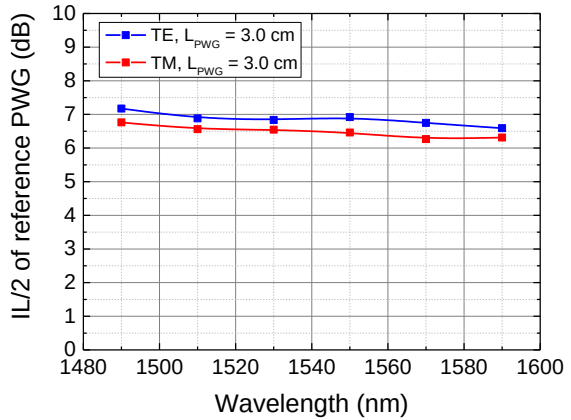
Insertion loss measurement:

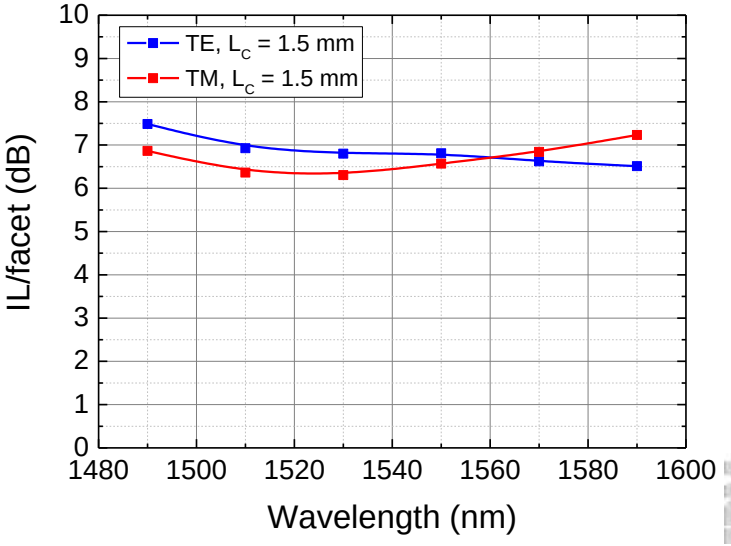
- Wavelength sweep over **C-band**
  - Full path vs ref. PWG path
- High PWG propagation loss



Schematic view of Si-photonics chip assembled by flip-chip bonding



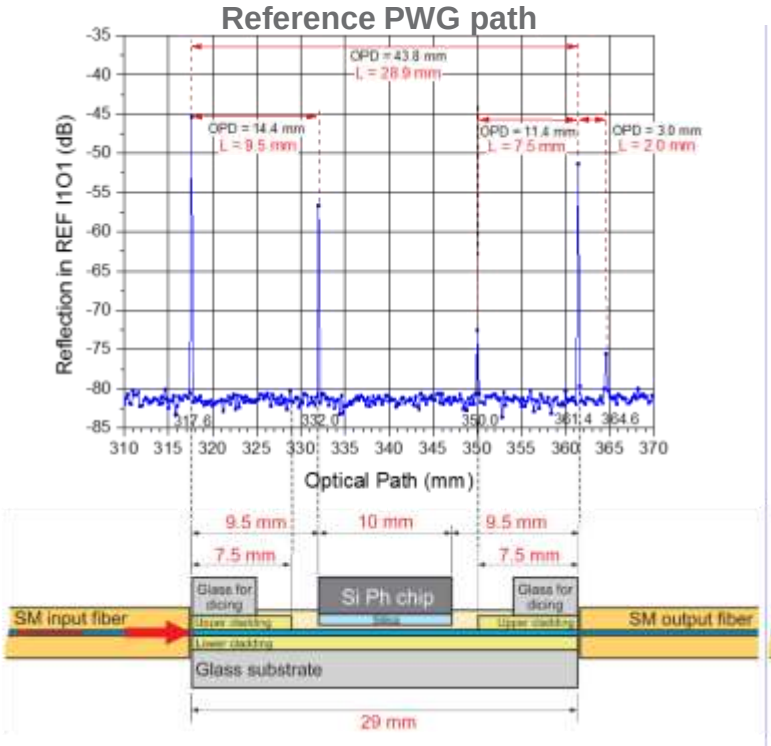


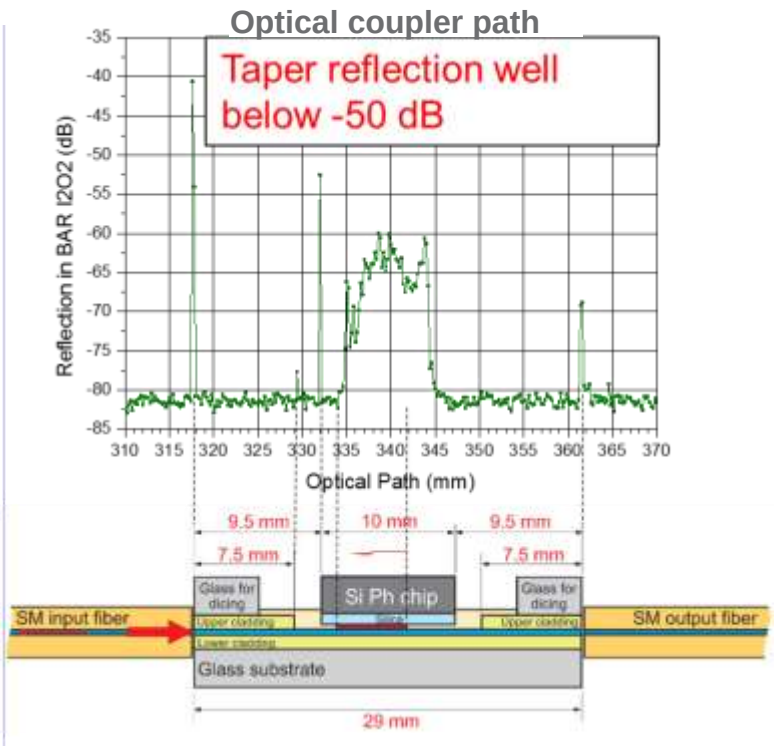


Optical back-reflection characterization

High resolution optical reflectometer measurement (HP 8504B)

- No significant back-reflections from the adiabatic coupler





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Summary

- Chip-level assembly of Si photonics onto the processor package
  - Offers a path to high bandwidth and low cost optical IO
  - A supply chain ecosystem has to be established

- Adiabatic optical coupling enables efficient, broadband and polarization tolerant chip to polymer waveguide interfacing
  - Compatible with existing electrical assembly processing steps

Path towards high-level of electro-optical integration & scalability

Acknowledgements

- Ralph Heller, Ute Drechsler and the other ZRL *BRNC team* members
- Nicholas Boyer, Paul Fortier @ IBM Bromont

- Dow Corning Corporation for the polymer materials support

- EU co-funded projects
  - FP7: CARRICOOL
  - Horizon2020: WIPE and STREAMS

- ..thank you

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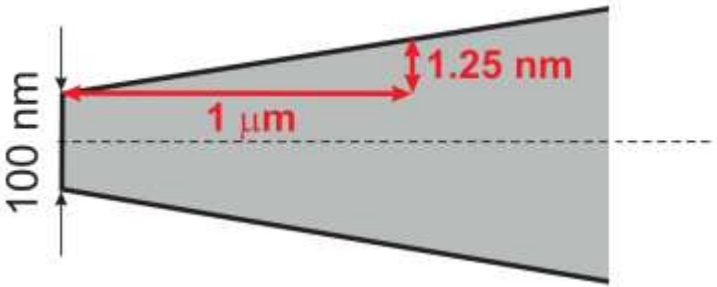
Back-up slides

On:

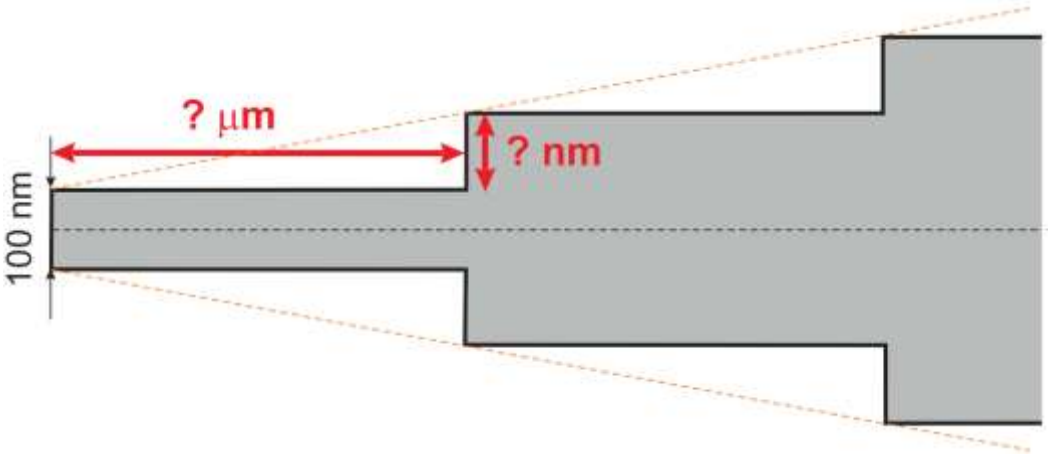
- PDL and wavelength dependent loss

Scattered loss for larger ebeam BSS

Design

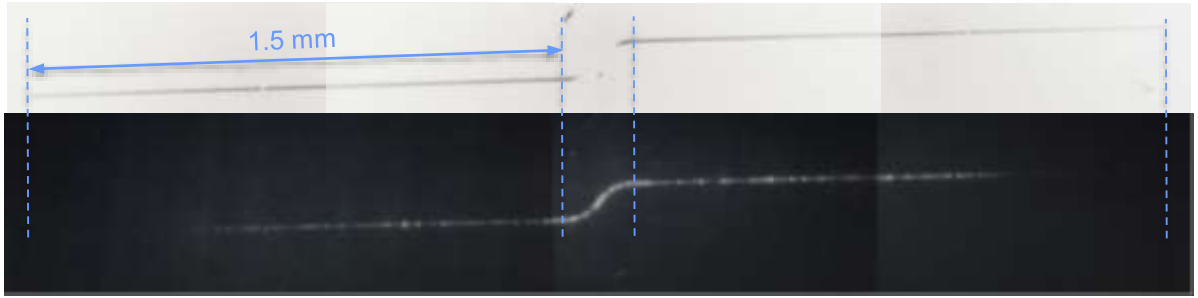


e-Beam writing



Scattered light of TE vs TM mode for larger ebeam BSS

TE
L_C = 1.5 mm
(Offset = 0 μm)



TM
L_C = 1.5 mm
(Offset = 0 μm)