Co-Design and Co-Integration of Photonic and Electronic Circuitry: the H2020 WIPE Approach

X. Yin¹, J.J.G.M. van der Tol², M. Matters², A. La Porta³, B.J. Offrein³, K. Solis⁴, T. Durrant⁴, V. Calzadilla⁵, F. Soares⁵, G. Coudyzer¹, J. Bruines⁶, J. Eisses⁷, J. Bauwelinc⁴¹

(1) IDLab Design, imec – Ghent University, 9052 Ghent, Belgium, E-mail address: xin.yin@ugent.be
(2) Technische Universiteit Eindhoven, P.O. Box 513, 5600 MB Eindhoven, The Netherlands
(3) IBM, Zurich, Switzerland
(4) Effect Photonics, The Netherlands
(5) Fraunhofer HHI, 10587 Berlin, Germany
(6) SMART Photonics, 5612 AX Eindhoven, The Netherlands
(7) Berenschot, 3503 RA Utrecht, The Netherlands
Outline

• Introduction
• EU H2020 [WIPE] Project: Wafer-scale Integration of Photonics and Electronics
• Wafer Bonding & Interconnects Technology
• Electronic – Photonic Circuitry Co-Design Flow
• Packaging and Thermal Issues
• Conclusion
The Connected Age

• Cloud & Internet of Everything ⇒ Higher data rate and more devices!

**By 2019:**

- More Internet Users
  - 2014: 2.8 Billion
  - 2019: 3.9 Billion

- More Devices & Connections
  - 2014: 14.2 Billion
  - 2019: 24.4 Billion

- Faster Broadband Speeds
  - 2014: 20.3 Mbps
  - 2019: 42.5 Mbps

- More Video Viewing
  - 2014: 67% of Traffic
  - 2019: 80% of Traffic

*Source: Cisco VNI Forecast, 2014-2019*
Clouds and Distributed Computing

• Huge growth in datacenter network bandwidth requirements
  – Photonics-Enabled Disaggregated Data Centers

• 400G or future Tb/s Ethernet
  – high serial rates for 500m and 2km single-mode fibre applications
  ⇒ lower lane counts, higher spatial efficiency

• Datacenter/HPC: optical interconnects are needed!
  – Low power consumption
  – Low cost solutions

Amin Vadhat, Google, Interop’16 Keynote
Transceiver Form Factors

Pluggable transceivers with varying dimensions and power classes

On board optics not included, specs expected later in 2017

Dimensions in mm

100G products

400G products

*Current commercial

Prof. X. Yin, imec - Ghent University, ACP 2017, Guangzhou
## Power Dissipation in 400G Modules

### Power Consumption Survey

<table>
<thead>
<tr>
<th></th>
<th>CFP8 8λ</th>
<th>OSFP/OSFP-DD 8λ</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHY</td>
<td>19%</td>
<td>25%</td>
</tr>
<tr>
<td>Driver</td>
<td>5%</td>
<td>7%</td>
</tr>
<tr>
<td>TIA</td>
<td>10%</td>
<td>13%</td>
</tr>
<tr>
<td>Misc.</td>
<td>16%</td>
<td>22%</td>
</tr>
<tr>
<td>(T/ROSA+TEC)</td>
<td>50%</td>
<td>33%</td>
</tr>
</tbody>
</table>

**Max:** 16W

**Integrated Electronics/Photronics promise footprint/power consumption improvements**
EU H2020 [WIPE] Project

WIPE in short

- Physical electronics-photonics (photronics) connection
- Novel co-design, connection and die attach flows
- Wafer-scale integration of silicon based electronic (Bi)CMOS and InP based photonic circuitry.
- 8 Partners and 2 Observers from Netherlands, Belgium, Germany, UK and Switzerland

http://wipe.jeppix.eu/about-us.html
# Partners in EU H2020 [WIPE] Project

<table>
<thead>
<tr>
<th>Participant No *</th>
<th>Participant organisation name</th>
<th>Acronym</th>
<th>Contributions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Eindhoven University of Technology</td>
<td>TU/e</td>
<td>Design and technology</td>
</tr>
<tr>
<td>2</td>
<td>IDLab, Imec - Ghent University</td>
<td>Imec</td>
<td>Electronic design</td>
</tr>
<tr>
<td>3</td>
<td>Effect Photonics Ltd</td>
<td>EFFECT</td>
<td>Testing</td>
</tr>
<tr>
<td>4</td>
<td>IBM Research GmbH</td>
<td>IBM</td>
<td>Optical interface, packaging</td>
</tr>
<tr>
<td>5</td>
<td>Fraunhofer Heinrich Hertz Institute</td>
<td>HHI</td>
<td>Photonic ICs</td>
</tr>
<tr>
<td>6</td>
<td>Smart Photonics B.V.</td>
<td>SMP</td>
<td>Optical couplers, dissemination</td>
</tr>
<tr>
<td>7</td>
<td>Berenschot Groep B.V.</td>
<td>BT</td>
<td>Project office</td>
</tr>
<tr>
<td>8</td>
<td>Effect Photonics B.V.</td>
<td>EPNL</td>
<td>Technological architecture</td>
</tr>
</tbody>
</table>

Observers:
- NXP (NL)
- Oclaro (UK)

WIPE Wafer Bonding & Interconnects

Hybridly integrated electronics and photonics on wafer scale → WIPE concept

a (Bi)CMOS-compatible way to attach a photonic layer to an integrated electronic circuit which is generic to many combinations of photonic and electronic wafers.
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WIPE Wafer Bonding & Interconnects

Processing at HHI
Single project wafer run
Polymer processing at IBM
SSC Waveguide definition
Flip InP
WIPE Wafer Bonding & Interconnects

BiCMOS wafer
Marker backside InP wafer
Bonding
InP Substrate removal
 WIPE Wafer Bonding & Interconnects

InP Substrate removal
InP Substrate removal
Bonding & Interconnects: Initial Results

• Bonding test: top view on the result after substrate & etch stop removal ⇒ no cracks visible

• Interconnects: process realized with multi resist layer deposition and Fluoride-based dry etch ⇒ resistance in the order of 100 mOhm/cm
Co-Design: Challenge and Opportunity

Prof. X. Yin, imec - Ghent University, ACP 2017, Guangzhou
Horizon 2020 contract number 688572

WIPE Co-Design Tool Development

Based on existing EIC and PIC design flows and its interfaces, considering packaging aspects

Platform selection

Specification

Building block/subcircuit design

Draft floor plan

Final layout

Verification

Packaging

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WIPE PIC Development

Gen. 0

Test Structures to evaluate process flow

Gen. 1

PD avoids back reflections to DFB

PD dark current thermometer

Heater tunes DFB wavelength

Building block: EML

Prof. X. Yin, imec - Ghent University, ACP 2017, Guangzhou
Test Structures to evaluate process flow

Optical Rx based on a rather conventional PIN photodiode (PD), connected to a SSC, BW > 35 GHz, 0.8 A/W at 1550nm

Building block: PIN-PD
WIPE EIC Development

Gen. 0
Calibration and Test Structures

Gen. 1
2-channel 56Gb/s PAM-4 EAM driver
2-channel 56Gb/s PAM-4 TIA receiver
WIPE Prototype Packaged Demonstrator

WIPE Approach: RF/Optical, Heatsinking and Packaging
WIPE Sub-assembly Design

- Potential to fit in a standard form factor (e.g. CFP8, OSFP, QSFP-DD)
- Eval kit will be designed (i.e. break-out board)
Sub-assembly Design: Mechanical

Mechanical scheme and design
- Photronic chip stack attached to the PCB using silver-filled epoxy resin for die bonding
- Heat sinks attached using the same resin or by solder
- Top heat sink only if strictly required
Sub-assembly Design: Optical Connections
SToA: Coupling between Si photonics chip and SM fibers

- **Challenge:** Spot-size conversion
- **Solution:** Adiabatic coupling
- **Advantages:**
  - High tolerance against positioning errors, Wavelength, Polarization
  - Low backreflection
  - Compatible with electrical assembly techniques

- **On-chip SOI waveguide**
- **Spot-size conversion**
- **Single mode fiber core**

0.5 x 0.2µm

Sub-assembly Design: Optical Connections
Experimental demonstration of adiabatic coupling

- Adiabatic coupling based on silicon waveguide tapering
- Polymer waveguide and silicon waveguide are in contact
- Reducing the silicon waveguide width forces the light to couple to the polymer waveguide

⇒ No additional components required
⇒ Optical connection established during soldering

Sub-assembly Design: Optical Connections

- Only one single-mode (SM) fiber required for, respectively, the TX and RX chip
- Optical signals guided at the edge of the photronic chip by the SSC
  - SSC converter matches the mode-size between the mode in the InP to the one of the SM fiber
- Fiber placement by active optical alignment and subsequent fixation by low-shrinkage UV-curable adhesive resin
Sub-assembly Design: Thermal

- Electronic IC needs to dissipate more power than the PIC
- PIC more temperature sensitive
- Polymer has low thermal conductivity
- Modeling with heat sinks attached, photronic assembled and attached to the PCB
- Heat maps:

![Power map of Rx chip, electronic layer contains all heat sources](image1)

![Power map of Tx chip, heat sources are present in the electronic and in the photonic layer](image2)
Sub-assembly Design: Thermal (Cont’d)

- Heat transfer coefficient 10.000 W/(m²K)
- Heat maps
  - at the device plane for the silicon chip
  - on the InP/polymer interface of photonic chip
- Averages and maxima relative temperatures are calculated over the entire Electrical IC and PIC

<table>
<thead>
<tr>
<th>#</th>
<th>layer</th>
<th>material</th>
<th>thickness [µm]</th>
<th>thermal conductivity [W/mK]</th>
<th>comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>130</td>
<td>heat sink top</td>
<td>Zn</td>
<td>2000</td>
<td>113-140</td>
<td>zinc die cast is standard for housing of QSFP connector</td>
</tr>
<tr>
<td>120</td>
<td>TIM top</td>
<td>TC 5622</td>
<td>20</td>
<td>4.3</td>
<td>Thermal Interface Material, Dow Corning thermal paste</td>
</tr>
<tr>
<td>110</td>
<td>polymer</td>
<td>Dow Corning</td>
<td>20</td>
<td>0.35</td>
<td>thermal conductivity ~25% of SiO2</td>
</tr>
<tr>
<td>100</td>
<td>InP</td>
<td>InP</td>
<td>15</td>
<td>68</td>
<td>layer in the device is structured and could be thinner 5µm</td>
</tr>
<tr>
<td>10</td>
<td>polymer</td>
<td>Dow Corning</td>
<td>10</td>
<td>0.35</td>
<td>thermal conductivity ~25% of SiO2</td>
</tr>
<tr>
<td>11</td>
<td>interconnect</td>
<td>Au</td>
<td>20</td>
<td>310</td>
<td>20x20µm cross section embedded in layer 10&amp;20</td>
</tr>
<tr>
<td>20</td>
<td>polymer</td>
<td>Dow Corning</td>
<td>10</td>
<td>0.35</td>
<td>thermal conductivity ~25% of SiO2, includes air gaps as thermal barrier</td>
</tr>
<tr>
<td>200</td>
<td>Si</td>
<td>Si</td>
<td>375</td>
<td>149</td>
<td></td>
</tr>
<tr>
<td>210</td>
<td>Ag filled epoxy</td>
<td>H2OE-HC</td>
<td>50</td>
<td>10.9</td>
<td>up to 23 W/mK if additional curing step of 1h@ 200°C</td>
</tr>
<tr>
<td>220</td>
<td>PCB</td>
<td>laminate</td>
<td>1000</td>
<td>17</td>
<td>laminate with filled thermal vias, 4.5% Cu fill fraction (first estimation)</td>
</tr>
<tr>
<td>230</td>
<td>TIM bottom</td>
<td>H2OE-HC</td>
<td>50</td>
<td>10.9</td>
<td>see #210, interface can be soldered e.g. In#227 54 W/mK, BL &gt;20µm</td>
</tr>
<tr>
<td>240</td>
<td>heat sink bottom</td>
<td>Cu</td>
<td>4000</td>
<td>384</td>
<td>new heat sink, would be part of the casing</td>
</tr>
</tbody>
</table>

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Thermal Simulations: TX Chip

Summary of simulation results:

• Top heat sink in the PIC TX is required

• Two heat sinks of 5,000 W/(m²K) each seems to suffice

Temperature map of one half of the Tx chip showing the electronic layer boundary (left) and the photonic layer boundary (right) applying a heat transfer coefficient of 10,000 W/(m²K) to the boundaries. $T_{\text{avg}} = 11.2$ and $9.4$. $T_{\text{max}} = 20.0$ and 37.3, 2°C distance between contour lines

2D plot of heat transfer coefficient sweep for the top and bottom heat sink up to 10000 W/(m²K) showing $T_{\text{max}}$. Left for the electronic layer and right for the photonic layer.
Thermal Simulations: RX Chip

Summary of simulation results:

- Top heat sink in the PIC RX can be avoided
- One (bottom) heat sink of 5,000 W/(m²K) seems to suffice

Temperature map of one half of the Rx chip showing the electronic layer boundary (left) and the photonic layer boundary (right) applying a heat transfer coefficient of 10000 W/(m²K) to the boundaries. $T_{avg} = 4.2$ and 3.1. $T_{max} = 7.5$ and 5.0 with 0.5°C distance between contour lines.

2D plot of heat transfer coefficient sweep for the top and bottom heat sink up to 10000 W/(m²K) showing $T_{max}$. Left for the electronic layer and right for the photonic layer.
WIPE Technological Architecture Outlook

Know-how to favour & enable technology adoption

Leveraging the disruptive technology

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Conclusion

• Effective co-design and co-integration of photonics and electronics allows for miniaturization and subsequently energy and cost savings.

• We describe the EU H2020 WIPE approach towards photonic/electronic integrated circuitry co-design/co-optimization and wafer-scale integration.

• Initial results are promising and the WIPE technologies have potential to enable next-level photonic/electronic integration.
Thank you for your attention

Any Questions?

Contacts:
• Email: Xin.Yin@UGent.be, Xin.Yin@imec.be