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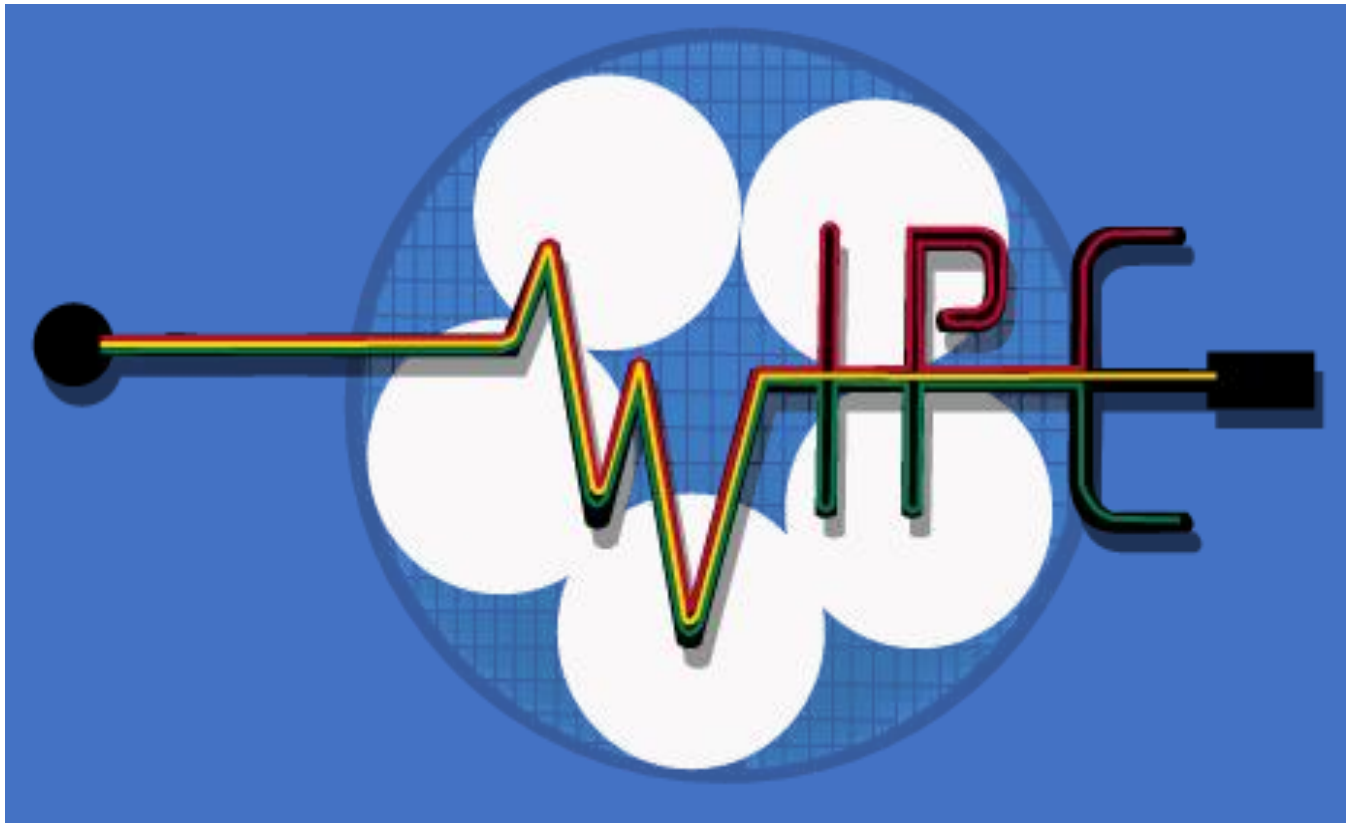


Wafer scale Integration of Photonics and Electronics

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 688572 (WIPE)

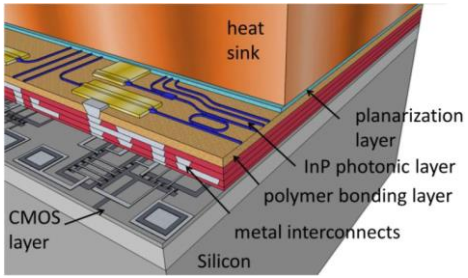
Context and Challenges

Data communication (Netflix, Facebook, Youtube, …) will increase 1000x in the coming 10 years, requiring the construction of many new mega data-centres loaded with interconnected computers.

Today's silicon technology based data centres already consume more than 3% of the world's energy production and are reaching their processing limits. Photonic IC's, that use light instead of electricity, match perfectly with the need for higher processing speeds and lower power consumptions. Photonic IC's still need electronic driver circuitry however and the connection between both circuit types currently is a major performance limitation and cost constraint.

WIPE in short

The WIPE project addresses the physical electronics-photonics (photronics) connection. It studies novel co-design, connection and die attach flows for wafer-scale integration of silicon based electronic (Bi)CMOS and InP based photonic circuitry.

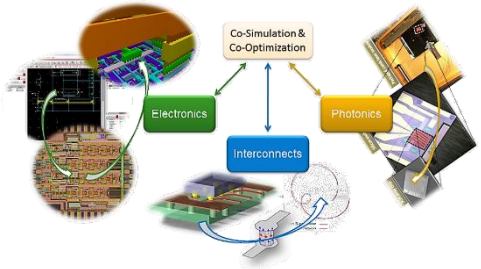


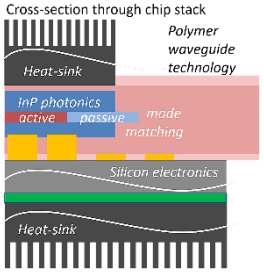
A schematic of the combined photronic IC's stack is shown in the figure.

Approach and Methodology

The **co-design of the electronic and photonic IC's** allows for optimization in area and power consumption, e.g. between de optical phase modulator and its electronic driver circuit.

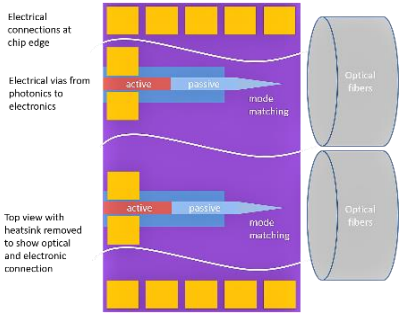
Significant **floor-plan reduction** Is obtained by replacing many thousands of square microns of bond pads with strip-lines of just a few microns squared. The **electronic connections** can therefore be extremely short, allowing for high frequency operation. Impedance matching can be re-engineered to improve both performance and power consumption.





Athermalisation is demonstrated by intimate short-loop control and on-chip temperature monitoring. The use of InGaAlAs active layers enables the gain elements to operate at the required higher temperatures**.**
Thermal cooling will be simplified by applying double sided elements with air-cooled die stack silicon heatsinks.

Optical connection is made easy by integrating in-plane mode expansion elements. The polymer layers used for wafer bonding will be combined with lower index cladding materials to serve both as encapsulation and as large cross-section out-coupling waveguides, enabling a route to mass manufacturable low-cost solutions.



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