Low Resistance Metal Interconnection for Direct Wafer Bonding of Electronic to Photonic ICs

A. Meighan, T. de Vries, E. Smalbrugge, M. Wale and K. Williams

Eindhoven University of Technology, 5612 AZ Eindhoven, the Netherlands

Wafer scale co-integration of electronic integrated circuits (EICs) and photonic integrated circuits (PICs) using the adhesion bonding technique may enable intimate integration and open up new opportunities for improved performance, power efficiency and manufacturability. Benzocyclobutene (BCB) polymer offers good adhesion, low dielectric constant and compatibility with Si and InP processing. In this paper, we present a method to create short gold vias through the BCB layer, demonstrating low-resistance break-free metal connection.

Introduction

The need for higher bandwidth optical links with lower power consumption is driving increasing levels of integration. Transmitters with multiple wavelength channels have been demonstrated on generic integration platforms [1] and with high data dates per wavelength on customized integration platforms [2,3]. However this leads to higher numbers of electrical connections per chip, motivating tighter integration between electronics and photonics [4]. In this work we describe a key enabling step towards ultra-tight electronic to photonic integration at wafer-scale.

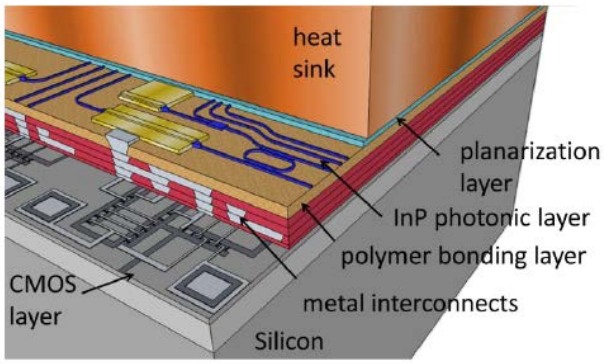

Figure 1. Schematic diagram of Photonic circuits integrated CMOS with wafer to wafer bonding

Wafer-scale electronic photonic integration

Fig.1 shows a schematic diagram for the chosen concept of electronic-photonic integration. The lower CMOS layer is shown with electronic driver circuits and a fully processed high-performance InP photonic layer that is aligned and attached with a polymer bonding layer. The substrate of the photonic circuit is removed, leaving a thin PIC structure with optical inputs and outputs. The electrical connection relies on the creation of metal vias through the polymer bonding layer between the silicon and InP. A polymer adhesion layer thickness in the range 2 to 30μm is typically required in order to obtain a mechanically sound structure with appropriate optical, electrical and thermal isolation.

In this work we study methods to create 2-D arrays of vias vertically through polymer. We compare three masking techniques for the creation of holes through thick layers of

BCB and validate the most promising approach by creating gold-plated vias. The resistance of the vias is measured with the four point probe method.

Masking and etching

Samples of cured BCB were prepared on top of three 2" silicon wafers. A thin 50nm SiO_2 layer was deposited by PECVD before spinning on 27µm layers of BCB, which were then cured at 270^o C for two hours. We tried to find how deep and smooth we can etch the BCB with three hard mask techniques. A mask with a range of openings from 116µm to 1250µm and a range of pitches with minimum opening separation of 25µm was used. Patterning was performed with three different hard mask approaches:

1- Silicon nitride mask: A 360 nm Silicon Nitride layer was deposited on top of the BCB by PECVD. A pattern of holes was etched on the silicon nitride layer by photolithography and plasma etching by combination of CHF_3 with flow of 50 Standard Cubic Centimetres per Minute (sccm) and oxygen with flow of 5sccm and power of 100W for 4 minutes.

2- Chromium mask: 100 nm of chromium was evaporated on top of the BCB and patterned with a lift off process.

3- AZ 9260 photoresist: 10µm of the positive photoresist was used as a mask and patterned during the lithography step. Post baking of the photoresist for 20 minutes at 110°C resulted in sloping side walls in the photoresist and these slopes are subsequently transferred from photoresist to the BCB.

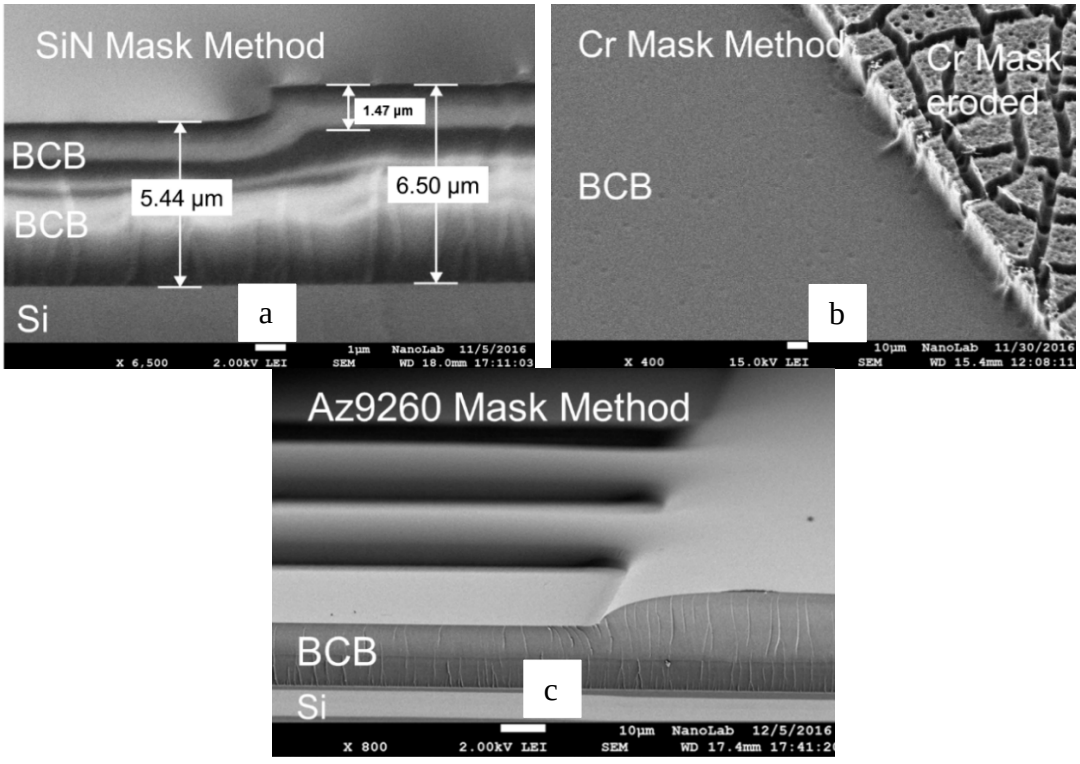

Figure 2. SEM images for three masking methods: a) Silicon nitride mask which is completely eroded after 1.2µm etch of BCB; b) Chromium mask showing stress induced cracking in the hard mask on the residual BCB; c) AZ 9260 photoresist which is consumed for 8µm etching of BCB

Via holes were created by reactive ion etching with the gas combination of SF_6 (gas flow = 6 sccm) and O_2 (gas flow =40 sccm) and forward power of 200W to achieve a high etch rate of 0.6µm/min. We continued etching until the mask was consumed completely and

we measured the step height of the etched BCB with a Tencor Profilometer to check how deep we can etch the BCB with each mask. Scanning electron microscope images of the results of the various masking techniques are shown in Fig 2. The silicon nitride mask is completely consumed for 1.2µm BCB etch depth (step height was measured after 5 minutes of etching), as shown in Fig 2(a). Fig 2(b) shows that the Chromium mask was consumed after etching 21µm of BCB (step height was measured after 35 minutes of etching), showing a higher selectivity of chromium against oxygen and SF_6 plasmas, but there is erosion which appears to come from cracks in the hard mask. The resilience of the AZ9260 resist was sufficient to allow etching of up to 8µm of BCB (step height was measured after 20 minutes of etching) with a single layer of resist mask (Fig 2(c)). We noted that the sloped side walls obtained with the AZ9260 mask would facilitate full coverage in the seed layer for plating when using the evaporation technique for metal deposition and AZ9260 resist was accordingly chosen for the subsequent work.

Metallization

Three samples with 4, 7 and 8µm of cured BCB were prepared on quarters of 2" Silicon wafers with the same 50 nm SiO_2 layer to enhance adhesion. AZ9260 was used as a mask for etching the BCB, resulting in sloping side walls. A thin seed layer of Ti/Au (50/100 nm) was then evaporated on the samples. In order to maximize coverage on the sidewalls, the carrier was tilted by 45 degrees and rotated during deposition. The via opening mask was offset by 50 µm to define vias on the side-wall. This results in the creation of metal tracks including vias in the end part. AZ4533 photoresist was used to define the areas for electro-plating in the gold plating bath with different potential cycles. After plating, the resist was removed by acetone and the seed layer was wet etched with cyanide-containing solution.

Referring to Fig.3 (a), the closest vias are 25µm apart with examples at 116µm shown in Fig.3 (b). This is a route to high-density integration. The cross-section image taken after focused ion beam (FIB) etching shows a break-free connection. A constant metal thickness of 1.2 µm is observed in the image over the slope. There is variation in plating thickness across the wafers of order 0.7 to 3.7 microns which is attributable to non-optimum sample sizes. Additionally, different numbers of potential cycles were used per sample in the plating bath.

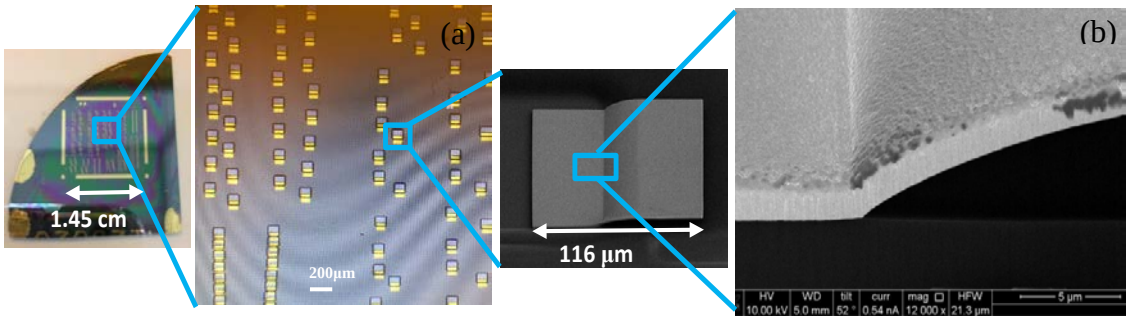

Figure 3. Metallization of 116x116 µm^2 through polymer vias on a quarter of a two-inch silicon wafer

Measurement

IV measurements were conducted on several hundred sites by scanning the voltage from 0V to 1V. All measurements were repeated at least twice and show consistency. Four-probe measurement was performed for different lengths of metal tracks, with and without vias. In theory the resistance of the tracks has a linear relation to resistivity (ρ) and length (l) and inverse relation to thickness (t) and depth (w) of metal:

$$R = \rho \frac{l}{w * t} \quad (1)$$

The resistivity of pure bulk gold is 2.44×10^{-8} Ωm and we used this value as an estimate for our plated gold layer. Fig. 5 shows the resistance as measured by the 4-point method versus separation between the probes. Measurement results consist of 49 data points across 3 samples. Open symbols in the graph are metal tracks without vias that are on top of the silicon and crossed symbols are tracks with vias from silicon to the top of the BCB layer. By using Eq.1 an estimate of resistance for the thinnest and thickest plated tracks has been calculated and these estimates are presented in the graph as the blue and red lines respectively. All measurement data lie between these two limits, both with and without vias, confirming negligible excess resistance from the vias. The thickness of BCB layer has no clear impact on electrical performance.

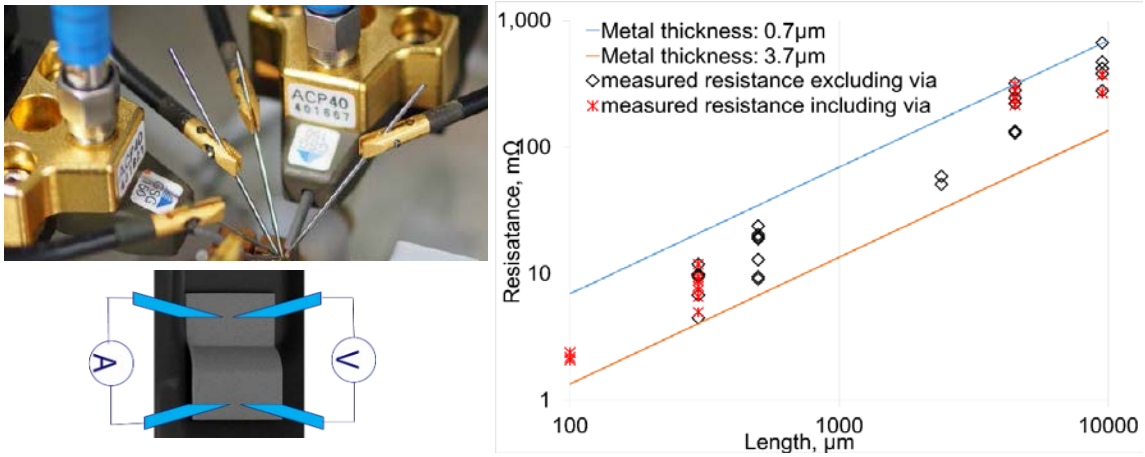

Figure 4. Four probe measurement across gold vias and also along lines without vias. No difference is observed between cases with and without vias. Resistance values lie within the predicted range.

Conclusion

In this paper we detailed the fabrication of wafer-scale low-mΩ resistance connections with 25-500µm separation and minimum 116µm dimensions. We demonstrate a method to create wafer scale grid array connections from top to bottom of a BCB layer, which is a promising candidate for electrical connection of PICs to EICs. Short high density connections will be important for defining low loss RF transmission lines on BCB.

Acknowledgment

The authors would like to thank Marion Matters-Kammerer, Xi Zhang and Xiao Liu from the MSM group of TU/e for their cooperation in this project and Weiming Yao and Jos van der Tol from PhI group of TU/e for helpful discussions. This research was carried out within the HTSM Photronics project, supported by the Dutch Technology foundation NWO.

References

[1] W. Yao, M. K. Smit, and M. J. Wale, “Monolithic 300 Gb/s Parallel Transmitter in InP-Based Generic Photonic Integration Technology,” IEEE Journal of Selected Topics in Quantum Electronics, vol. 24, no. 1, pp. 1–11, Jan. 2018.

[2] R. Maher, et al. “Constellation shaped 66 GBd DP-1024QAM transceiver with 400km transmission over standard SMF”, in 43rd European Conference on Optical Communication (ECOC), Gothenburg. Sweden, p.Th.PDP.B.2, 2017

[3] R.A. Griffin et al. "InP Mach–Zehnder modulator platform for 10/40/100/200-Gb/s operation", IEEE Journal of Selected Topics in Quantum Electronics, vol. 19, no. 6, pp.158-166, 2013

[4] R. Going et al. “Multi-channel InP-based Coherent PICs with Hybrid Integrated SiGe Electronics Operating up to 100 GBd, 32QAM” in 43rd European Conference on Optical Communication (ECOC), Gothenburg. Sweden, p.Th.DPD.C.3, 2017