

# Prospects for Electronic Photonic Integration

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**Abstract:** As InP integrated photonic circuits increase in complexity, component density, and circuit performance, electronic circuits need to be positioned ever-closer. We review the challenges and potential advantages for intimate electronic wafer to photonic wafer assembly.

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## 1. Monolithic circuits using InP integration photonic platforms

The number of photonic devices which can be realistically integrated in one photonic chip continues to increase as fabrication processes, enabling building blocks and design know-how mature. Photonic integrated circuits have now been demonstrated with tens and hundreds of active devices for tunable lasers [1], optical packet switches [2], and multi-wavelength transmitter circuits [3] and emerging PIC-enabled products place continued pressure on cost, energy efficiency, footprint and performance.

In the early stages of microelectronics development, year on year performance improvements were achievable in a cost effective manner through increases in chip area, feature size reduction, and the elimination of non-functional area [4]. Equivalent trends are evident in integrated photonics today:

Chip areas increase as more data modulators are added, and additional wavelengths are brought on chip [3]. Additional functions such as polarization management [5], switching and filtering functions [2] enable higher level functionality. The numbers of photonic devices are observed to rise exponentially [6]. Reticule sizes for defining the circuit features are limited only by the tooling developed for the electronics community, and this still surpasses the chip footprints typically used in photonics today.

Feature size reductions exploit enhanced optical confinement through deep-etched air-, dielectric, InP- or polymer-clad waveguides in the lateral plane, and substrate-isolated photonic circuits such as Silicon on Insulator or InP membrane on Silicon platforms in the vertical plane. Semiconductor lasers are typically 200  $\mu\text{m}$  and longer for wide tunable lasers, but these can be advantageously reduced to order 100  $\mu\text{m}$  within integrated circuits [7], and techniques to create 10  $\mu\text{m}$  and sub- $\mu\text{m}$  electrically pumped lasers and light sources [8] are actively being studied for further performance improvements. Substrate removal has the additional benefits of enabling low electrical parasitics [9] and improved optical crosstalk.

Eliminating non-functional area is essential to footprint reduction but leads to profound challenges in terms of optical, electronic [10] and thermal [11] crosstalk as well as optical, electrical and thermal connectivity as information density increases and heat transfer must be more efficiently managed. Nonetheless, monolithic photonic integration offers the powerful advantage of seamless coupling light between active and passive components with differing bandgaps and function with zero-length butt-joint interfaces and the smallest areas. Implementing the full photonic circuit prior to assembly enables wafer scale test and avoids assembly defined interfaces and parasitics within the photonic circuit [12].

These trends continue to put pressure on the electronic connection density, thermal management and optical connections, requiring innovative new methods for PIC assembly. The connections between electronic and photonic chips are particularly challenging, driving new thinking in the intimate connection between ICs.

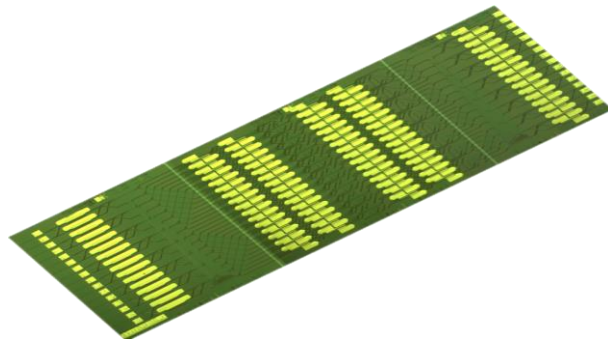


Figure 1: Example of a photonic integrated circuit for optical packet switching with 192 electrodes requiring GHz bandwidth electrical actuation [2]. Increasing levels of circuit complexity motivate intimate electronic integration.

## 2. Integrating electronics and photonics

A broad range of strategies have been identified for the chip and wafer scale connection and integration of photonic and electronic circuits, ranging from the full embedding of a subset of key photonic functions into electronics, through to 3-D integration, hybrid integration and heterogeneous integration. The possibility for wafer scale heterogeneous integration of photonics and electronics offers a particularly attractive means for systems integration. Table 1 offers an overview of the potential and challenges for these approaches.

Table 1: Convergence of electronic-photonic integrated circuit technologies

	Optical connections	Electronic connections	Thermal connections	Scaling potential
Monolithic electronic photonic integration	✗ Off-chip laser no amplifiers	✓ Ultrahigh density (FEOL)	✓ Silicon heatsink	✓ Embedded in electronics
3-D integration technology	✗ Off-chip laser no amplifiers	✗ Bond pad limited	✗ Silica insulator	✗ Assembly challenges
Hybrid integration Chips on carrier	✗ Optical vias at the assembly interface	✗ Bond pad limited	✗ Silica insulator	✗ Assembly challenges
Heterogeneous InP and electronics integration	✓✓ On-chip laser and amplifiers	✓ High density	✓ InP heatsink	✓✓ Energy efficient InP optoelectronics

Considerable effort has addressed integration of photonic circuits directly in electronic circuits. Modulators and detectors have been implemented with ring resonators in bulk silicon to compensate the efficiency ensuring an integration scheme which does not compromise the transistors [13]. Epitaxially grown Ge detectors have been embedded within silicon for enhanced efficiency at Front End of Line (FEOL) with deposition before the transistor anneal steps [14]. Receivers with integrated transimpedance amplifiers and detectors have been demonstrated with bandwidths to 56Gbit/s [15] in BiCMOS. Integration with the most advanced nodes has proven challenging due to size mismatch and the impact of photonic devices on transistors [16]. Silicon Photonic platforms do not currently support a viable way to include lasers or amplifiers. A number of researchers argue that a partition of light generating devices and the remaining photonic circuit is analogous to the partitioning of power supply and processor in electronics. This approach does however transfer design challenges from wafer scale processes to the package level, impacting the scalability. Silicon on Insulator substrates allow photonic circuits to exploit high confinement for a reduction in the waveguide cross-section. Additionally this enables vertically coupled integration with InP photonic devices. The hybrid integration of InP die with Silicon on Insulator photonic circuits does however make intimate integration with electronics more challenging and the use of a less widely used substrate reduces the motivation [13]. Much of the research focus for electronic photonic integration has instead addressed hybrid assembly of light-source free circuits using through silicon vias and flip chip assembly [17,18].

Co-designed photonics and electronics is enabling a step change in both efficiency and function. The shorter connections between detectors and amplifiers enable lower parasitic loss [18] and energy-efficiencies through a removal of resistive impedance matching. The closer placement of electronic and photonic chips already allows for higher numbers of electronic connections and functions such as digital to analog conversion to be performed in the optical domain [19,20]. So far these techniques have been studied for single elements and devices, enabling connections between co-designed chips which are placed side by side. The next logical step in integration would be parallel circuits, but this calls for a faster scaling in wiring density between the photonic plane and the electronic plane.

Membrane-based photonic integrated circuits offer a powerful means to create a photonic plane over an electronic control plane and therefore interconnection across the full surface of the photonic circuit. As the light source and full photonic functionality is maintained within the same plane, the photonic circuits can be created without compromising the electronics. Similarly the electronic fabrication flow is not compromised by the electronics. Powerful platforms including a range of lasers, high speed detectors and passive components are under development [9, 21-23], providing not only a route to electronic-photonic integration at the wafer scale, but also a scalable roadmap towards electronic-nanophotonic integration [8]. The recently awarded WIPE program which aims to achieve intimate integration for industry sources InP PICs and electronics circuits will also be presented [24].

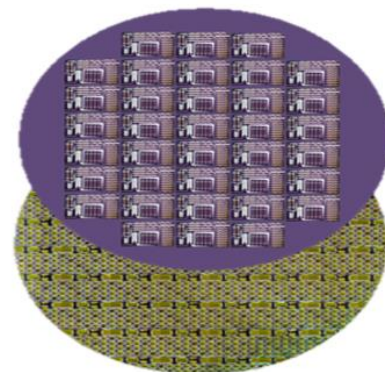


Figure 2: InP photonic wafer attachment to electronic wafer to enable intimate, high density

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