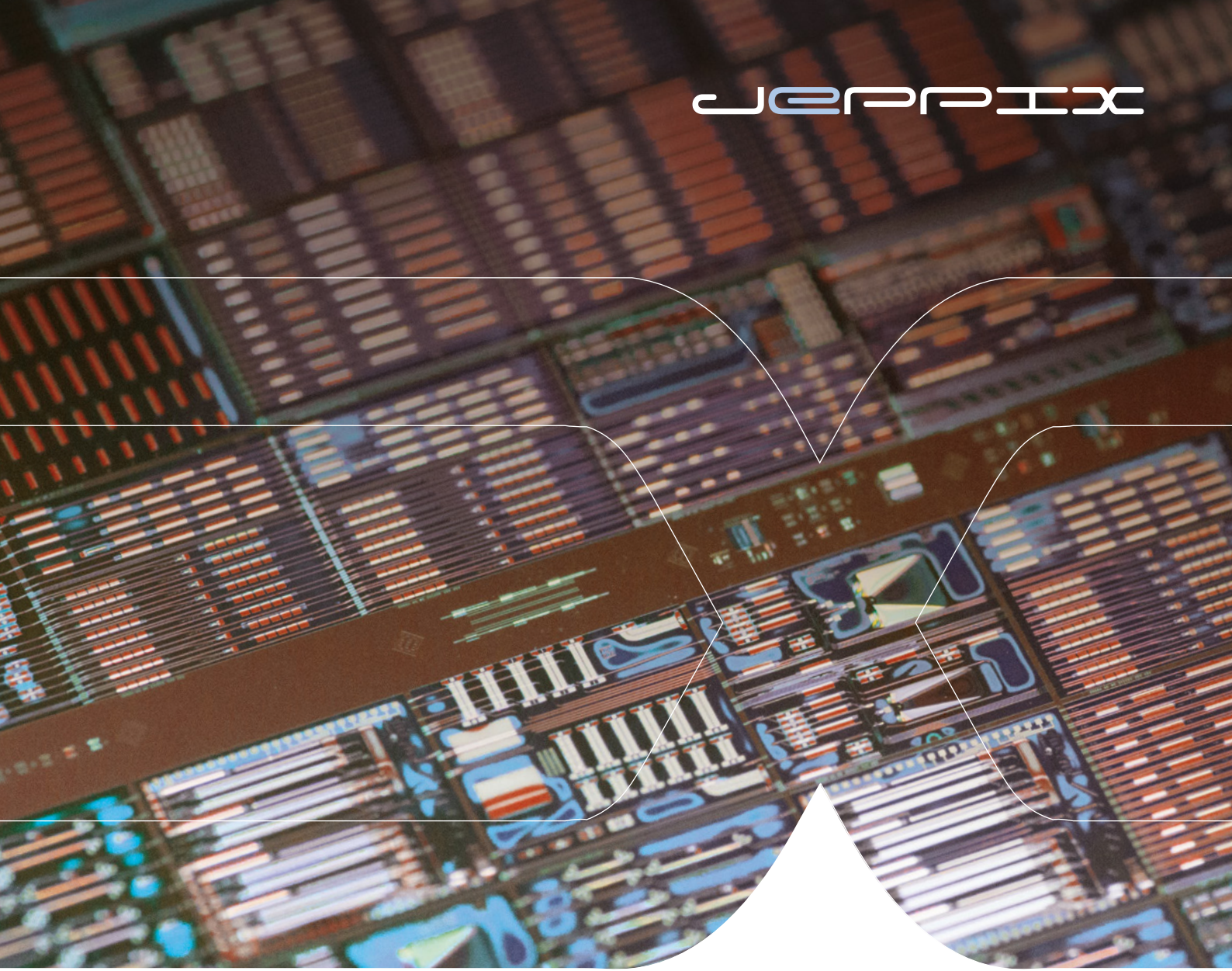
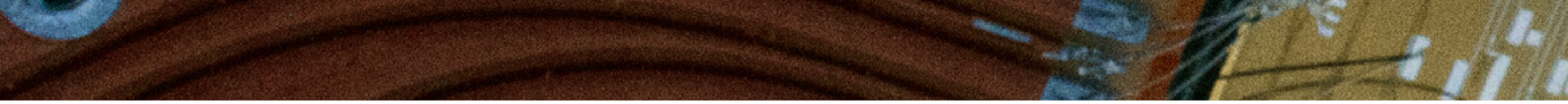


JePPIX ROADMAP 2018

THE ROAD TO A MULTI-BILLION EURO MARKET IN INTEGRATED PHOTONICS



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JePPIX is hosted by the Photonic Integration Technology Centre | www.pitc.eu

Executive Summary

InP-based Photonic Integrated Circuits (PICs) have become firmly established in the market place. InP PIC-enabled transceivers accounted for a 1B$ market share in 2015 and are expected to grow beyond 3 B$ in 2020. Today the application of PICs is broadening to other markets like fibre sensing, medical diagnostics, automotive (LIDAR) and metrology. JePPIX[1] partners SMART Photonics, Fraunhofer HHI and LioniX International are stimulating this development by offering cost-effective open access to advanced PIC foundry processes in InP and silicon nitride technologies. These photonics companies are the core of a vibrant and growing ecosystem, working in important markets in which Europe holds a lead. The JePPIX organization plays a key role in organizing this eco-system.

Since 2015, JePPIX has moved from EU-subsidized access to a commercially priced service and after an initial dip the increased awareness and enthusiasm for the technology has enabled JePPIX to manage this transition with an increase in use from businesses. In 2017 alone more than 60 different PIC designs were fabricated in 9 multi-project foundry runs, of which more than 30% were for industrial users, and strong business uptake is foreseen in the next 2-5 years. This roadmap addresses the issues of market expansion, including training and capacity planning needed to support that demand.

For this 2018 edition of the roadmap, JePPIX has carried out a survey of expert users in order to gauge user requirements and the need for technology developments going forward. Both InP-foundries, SMART Photonics and Fraunhofer HHI, currently offer a full suite of components including high-performance SOAs, lasers, modulators, detectors and a range of passive components. The technology roadmap includes improving component performance to support higher Baudrates (up to 56 GBaud/s), lowering propagation losses, and improving passive component performance by using 193 nm DUV lithography. A continuous effort is foreseen on improving the reproducibility of the processes. For further improvement in performance, a PIC fabrication roadmap is defined for improving the quality of epitaxial growth and adaption of fabrication equipment to the wafer size and mechanical

1 JePPIX: Joint European Platform for Photonic Integration of Components and Circuits, www.jeppix.eu

properties of InP wafers. This edition of the roadmap also looks further ahead to the arrival of future nodes supporting the integration of photonics and electronics on which several research projects are already running.

The silicon nitride foundry, LioniX International, offers its low-loss SiN integration platform (TriPleX) with a variety of passive components and thermal phase shifters, not only for the infrared but also for the visible spectral range. The technology roadmap foresees further lowering of the propagation losses, the adding of low-power stress-induced (PZT) phase modulators and extending the platform capabilities by hybrid integration of InP and TriPleX PICs. LioniX is also starting to provide open access to its visible light process, to cover applications outside the communications space, including bio photonics and virtual reality.

All three foundries have a Process Design Kit (PDK) with a range of building blocks that can be used by designers, freeing them from the underlying details of the technology. In cooperation with the JePPIX software partners the contents of the PDKs will be substantially extended to include statistical data for component performance and process tolerances. Further, more emphasis will be put on adding manufacturing rules in the PDKs, and to enable the design software to perform automatic Design Rule Checking (DRC) to reduce the chance of designer mistakes. The contents of building block libraries will be extended and an important development is the so-called PDAFlow API, an interface that enables interoperability between different software tools.

The development of reference packages for prototyping and low-volume production of PICs which are designed according to packaging templates with standardized positions for the electrical and optical ports, is seen as crucial to the development of the PIC market over the next few years. This standardization will also support prototype testing at affordable cost. JePPIX and some of its partners are participating in the PIXAPP Packaging Pilot Line with the ambition to define standardized packaging and test templates and to develop largely automated testing of compliant PICs. The standards are designed such that they support scaling to higher volumes.

The 2018 roadmap synthesizes JePPIX's analysis of the PIC market and market requirements for the coming 2-5 year timescale. Important technology developments required to foster the foreseen market growth are analyzed in many areas, including fabrication processes and equipment, design software, packaging and testing. JePPIX members are also contributing to the AIM roadmapping initiative led by MIT and the World Roadmap for Integrated Photonics, led by Photon Delta.

1. Introduction

JePPIX ROADMAP 2018

The PIC-market is rapidly growing, mainly driven by today's 100-400 Gb/s transceivers for telecommunications and datacenters, but other applications will benefit increasingly from the progress in PIC-technology. Four major platform technologies today are Indium Phosphide (InP), Silicon Photonics (SiP), Silica (SiO_2 or PLC) and Silicon Nitride (SiN).

JePPIX, the Joint European Platform for Photonic Integration of Components and Circuits, is a consortium in which Europe's key-players in InP and SiN-based Photonic Integration are cooperating to establish a technology infrastructure for cost-effective open access to standardized (generic) high-performance photonic foundry processes[1]. JePPIX started in 2006 as an open-access technology platform in the European FP6 Network of Excellence ePIXnet. The JePPIX consortium now covers the full chain of PIC-development and manufacturing, it includes partners for chip-manufacturing, PIC design tools and design services, packaging, testing and technology R&D, and it is active in stimulating business development with a large number of companies and researchers being supported by the consortium.

JePPIX is organizing commercial access to its foundry platforms in so-called Multi-Project Wafer runs (presently 11 MPW-runs per year), in a similar way as has been organized in microelectronics since the early eighties (e.g. MOSIS[2] , Europractice[3]). The first JePPIX MPW runs were performed by the COBRA research institute, now the Institute for Photonic Integration (IPI) at TU Eindhoven. Two major European projects started in 2009 and 2010 to transfer the generic foundry approach from the university environment to the industrial platforms of the company Oclaro and the Fraunhofer Heinrich Hertz Institute (HHI). In 2013 the company LioniX joined JePPIX with its silicon nitride (TriPleX) platform. The COBRA process was licensed to the startup company SMART Photonics. JePPIX now provides access to two InP-based foundry platforms (SMART Photonics and Fraunhofer HHI) and one silicon-nitride platform (LioniX International). JePPIX foundries have processed over 400 PIC designs in more than 40 MPW-runs over the last ten years.

1 M. Smit et al., An introduction to InP-based generic integration technology, Semicond. Sci. Technol. Vol 29 (2014) 083001.

2 www.mosis.com

3 www.europractice-ic.com

JePPIX has been publishing a roadmap for InP and SiN (TriPleX) based foundry technology approximately every two years (2012, 2013, 2015, and now 2018) and the next edition is planned for 2020. In our 2012 roadmap we predicted that the market for Photonic ICs would exceed 1 B€ before 2020. A recent market report[1] predicts that in 2020 the PIC market will be close to 4B€. Since our previous 2015 edition, we have observed a rapid increase in the use of Photonic ICs for high-speed (100+ Gb/s) transceivers. The transceiver PIC-market is strongly dominated by InP-PICs, and Silicon Photonics products are now becoming established as well, with opportunities opening up for Silicon Nitride. For the coming years the market prospects for these technologies look very good. Silicon Nitride platforms are expected to have impact in particular in biophotonics and microwave photonics.

In the past years we have seen a significant expansion of the PIC ecosystem, with a high number of companies actively exploring the impact of PIC technologies for their own businesses. This will be described in more detail in **chapters 2 and 3**. **Chapter 4** describes the market roadmap. For the InP-based foundries, the development of open access technology has been slightly slower than predicted in our 2015 roadmap. Despite this, most of the roadmap targets for 2016 have been realized and work on the 2018 targets is making good progress. The anticipated InP Pilot Line from the Horizon 2020 program is now expected to start in 2019. In **chapters 5 and 6** we will give a detailed update of the expected progress. The update is based on what we consider technically feasible in combination with the outcomes of a recent survey of user requirements. A summary of this survey is included in Annex 2 to the present roadmap. Progress and required developments of the design software and design resources are discussed in **chapter 7**. Important progress is presently being been made in the field of packaging and testing through cooperation with the PIXAPP Packaging Pilot Line[2] coordinated by JePPIX partner the Tyndall Institute. Packaging and module building are often the first consideration in the adoption of PIC technology and developments in this area are discussed in **chapter 8**. **Chapter 9** describes the required developments in wafer processing equipment. The cost roadmap that we published in 2015 has raised a lot of international attention and discussion. In **chapter 10** we will give an update of this roadmap.
Chapters 11 and 12 address the requirements for Public-Private funding and for education and training of the scientists and engineers that will be needed to support the expected rapid growth of the field in the coming years.

1 Lightcounting Market research, Integrated Optical Devices, 2016.

2 www.pixapp.eu

2. Applications Roadmap

So far telecom and datacom applications have been the main driver for the development of PIC-technology. According to market research by LightCounting[1] InP PIC enabled transceivers already accounted for a 1 B€ market share in 2015 and will grow to 3 B€ in 2020. Due to their increased performance and potential for low cost, the use of PICs is now broadening to other application fields representing a significantly larger market.

PICs?	Market Segment 2015	%	B€
YES	Production Technology	6	26,1
YES	Measurement & Image processing	7	33,2
YES	Optical Components and Systems	5	24,1
YES	Safety and Defence Technologies	7	30,2
YES	Medical Technology & Life Science	8	33,8
YES	Communication Technology	5	22
YES	Information Technology	16	71
NO	Displays	26	117,6
NO	Light Sources	7	33,4
NO	Photovoltaic	11	49
	Total photonics market value	**100**	**447**

Table 1 *Market share of the most important application fields.*

Table 1[2] lists the current market share for the most important application fields in photonics and indicates in which fields photonic integrated circuits could apply.

1 Lightcounting Market research, Integrated Optical Devices, 2016.

2 www.photonikforschung.de/media/branche/pdf/UT_Photonik_Handout_English_bf_abA7.pdf

Michael Lebby , CEO Lightwave Logic
"There is no doubt that integrated photonics rather than electronics is going to be key to the solution as Moore's Law for electronics begins to saturate. Beyond Moore's Law, we will require huge volumes of reliable, integrated photonic components in optical transceivers over the next decade."

Boudewijn Docter , CTO EFFECT Photonics
"The key enabling technology for DWDM systems is full monolithic integration of all photonic components within a single chip and being able to produce these in volume with high yield at low cost, and this is possible with an InP technology platform".

Martin Schell, Executive director Fraunhofer HHI
"Generic InP technology makes it possible for us to serve many different customers with development of PIC-prototypes without major investments for those customers. The separation of design and process lowers the entry hurdles significantly, which is especially important for our non-PIC-savvy partners e.g. from sensing applications."

José Capmany, Universitat Politècnica de València
"Microwave photonics is evolving from solely defense applications, to encompass civil scenarios through 5G communications, IoT and body/personal area networks. Generic integration InP technologies allowed our group to demonstrate integrated μwave photonics chips, with functions otherwise not possible with discrete components such as beat filters and opto-electronic oscillators."

Martijn Heck, PICs group, Aarhus University
"The new eco-system of design software, process design kits and multi-project wafer foundry services, as spearheaded by JePPIX, has enabled a whole new scientific field. Instead of optimizing your photodiode or laser diode by redesigning the epitaxial layer stack, for example, we can now focus on the design of the circuit. This implies that more complex applications are now becoming possible. Moreover, our technology is now closer to the industry, enabling technology transfer out of the lab."

Figure 1 *3" wafer fabricated on the InP generic technology platform of SMART Photonics. Image by F. Lemaitre.*

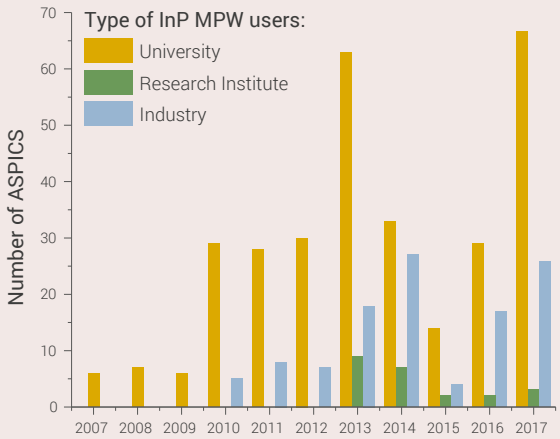

Figure 2 *Number of ASPICs fabricated per year (sorted by tape-out date).*

We expect that Photonic ICs will be increasingly applied in the fields of Production Technology (for metrology), Measurement, Optical Components and Systems, Safety and Defence Systems, Medical Technology and Life Science, Communication and Information Technology. In total they cover more than 50% of the total photonics market. In these novel application fields there is a huge potential for both small and larger companies to introduce novel or improved products, equipment or services which use Photonic ICs. We expect that these application fields will lead to a significant increase in the market share of PICs.

Without an open-access foundry infrastructure the costs for developing a PIC are prohibitively large for small companies and universities, and they also form a barrier for larger newcomers in the field that would like to start exploring the potential of PICs without major upfront investments. The open access foundry model used by JePPIX leads to a more than ten-fold reduction of the prototype development cost by sharing the costs of wafer fabrication by many users. Figure 1 shows a 3" wafer, fabricated with the InP generic platform technology of SMART, which shares PIC designs of more than 10 users. Since 2006 the JePPIX foundries have processed more than 400 Application Specific Photonic ICs (ASPICs, see Figure 2). More than 140 were fabricated in the last two years, for applications in telecommunications, data communications, fibre-to-the-home, fibre sensors, gas sensing, medical diagnostics, and metrology. Most of the designs were submitted by Universities, but a rapidly increasing part is coming from companies, most of them SMEs. Examples of fabricated PICs are shown in Figure 3, some of them are discussed in more detail on the next page.

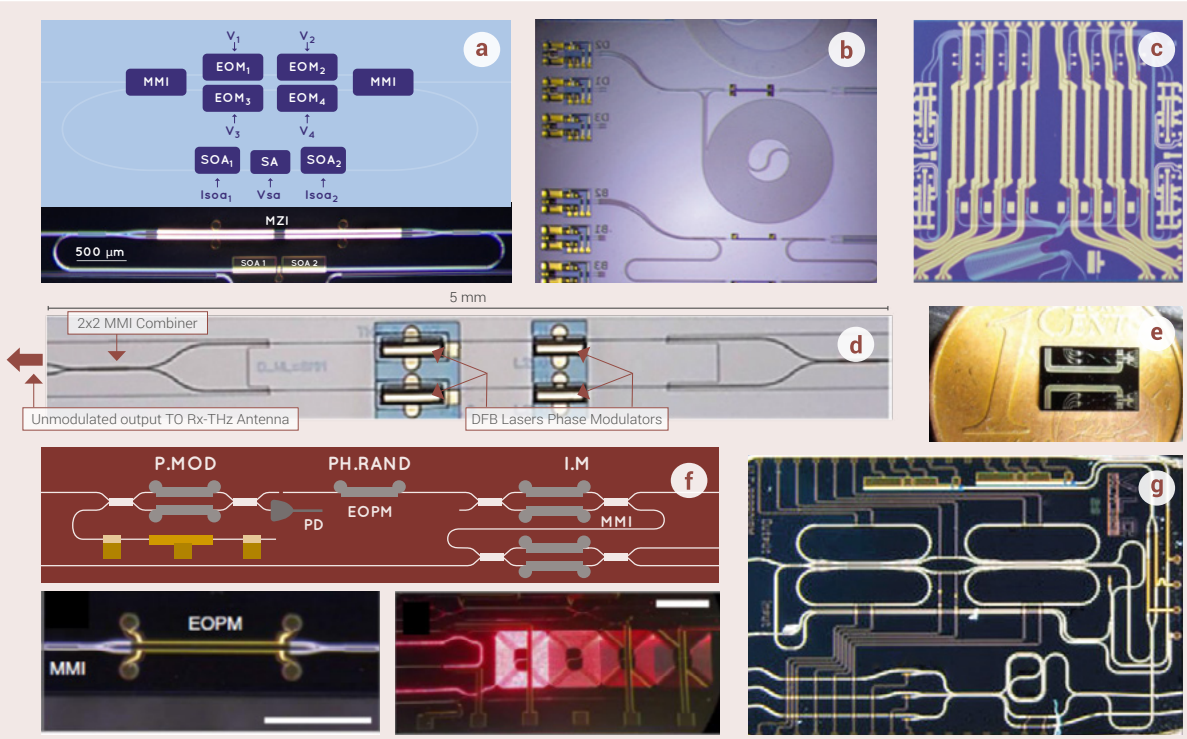

Figure 3 *Examples of ASPICS realized for a variety of application fields.*

- ***a*** *Optical frequency comb generator.*
- ***b*** *Read-out chip for a 4 channel FBG strain sensor for sensing applications.*
- ***c*** *320 Gb/s WDM transmitter for high-speed data communication.*
- ***d*** *Optical THz source for security scanning applications.*
- ***e*** *Quantum random number generator for quantum security.*
- ***f*** *Quantum key distribution, can be used for security protocols.*
- ***g*** *Microwave photonics filter for RoF (radio over fibre) applications.*

Datacom and Telecom

Datacom and telecom are currently the dominant application fields for PICs. High capacity data transmission is important for communication within and between datacentres. The generic monolithic InP open access technology offers the possibility to integrate one or more lasers in a single chip with passive waveguide devices and high-performance modulators and photodiodes, thus reducing the cost of assembly and packaging.

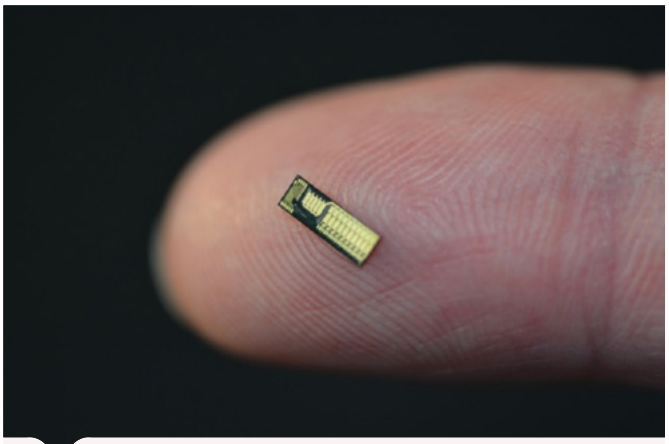

Figure 4 *100 Gb/s transceiver chip, EFFECT Photonics.*

EFFECT Photonics[1], a start-up in the field of high-speed communication, has developed powerful DWDM optical systems in single-chip technology. One of EFFECT's main products is shown in Figure 4. It is a 100 Gb/s transceiver made of an array of lasers stacked in parallel and connected to MZ modulators that are connected to an AWG which combines the different signals in a single waveguide which is fed to a booster SOA and then connected to an output fibre. DWDM systems are needed to cope with the increasing necessity of speed and bandwidth for data and telecommunications. The EFFECT products have been developed in a generic process, and have been optimized by customization of the generic process. Such a customization becomes an attractive option for the generic process when larger markets are to be addressed.

Sensor readouts

Sensor systems based on fibre Bragg grating interrogators represent a big market in photonics. They have a wide field of applications in terrestrial and aerial transportation, in astronomy and health monitoring. They are attractive because of their reliability, reproducibility, compactness, light weight, immunity to electromagnetic interference and low power consumption. Figure 3b shows a read-out chip for a 4-channel FBG strain sensor developed by the company Technobis on the HHI platform. The device measures a wavelength shift of a fibre Bragg grating in the 1465-1620 nm window. Sub-femtometer resolution is feasible at a sampling rate of 10 kHz. This is several orders of magnitude better than commercially available small-sized wavelength meters.

1 www.effectphotonics.nl

Other Applications

Photonic Integrated Circuits are becoming increasingly important for automotive applications, for example in LIDARs for drones or self-driving cars. InP PICs have the potential to integrate large numbers of optical amplifiers and phase modulators which are important in beam-steering arrays for LIDARS, they have the potential to replace today's more bulky and costly LIDAR systems.

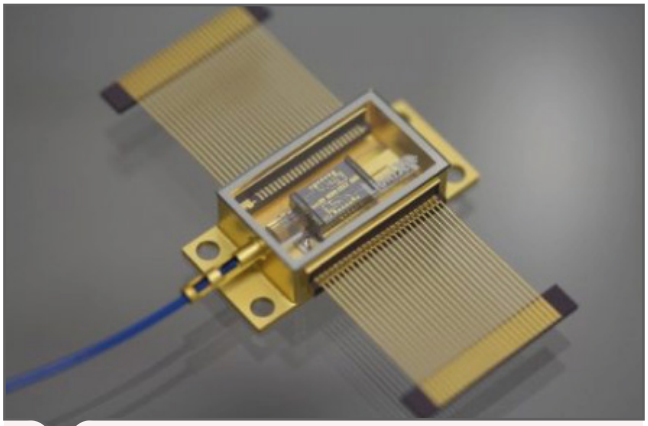

Figure 5 *Ultra narrow bandwidth tunable laser in a hybrid TriPleX technology platform. In the chip, a laser-gain section is hybridly attached to a tunable reflector, creating an external-cavity laser. The InP chip contains the first mirror and the gain section, the silicon nitride based TriPleX chip acts as a tunable wavelength-dependent mirror.*

For medical applications PICs for Optical Coherence Tomography (OCT) have gained a lot of attention since they can integrate a large part of the sensor system on single a chip, thus massively reducing its size making the device more practical and less aggravating to the patients.

Other emerging application areas are in agriculture where PIC-based spectrometers can be used to analyse the condition of seeds, fruits and vegetables. PIC technology enables low-cost gas sensors for monitoring CO_2 or other type of gases like the levels of methane emitted by the kettle.

We foresee also promising applications by combining InP and TriPleX platform capabilities. As described in Section 5 research is underway to enable low-cost precision-assembly of InP and TriPleX chips which will bring us a hybrid platform technology in which we can combine the active functionality and high-speed operation of InP technology with the low-loss capabilities of the TriPleX platform. Figure 5 shows an example of a tunable laser fabricated in the hybrid TriPleX technology platform of LioniX. It contains an InP-based optical amplifier fabricated on the HHI platform, which is hybridly coupled to a tunable TriPleX reflector circuit.

3. Business Roadmap

The sustainability of open access photonic integrated circuit technologies requires a combination of competitive industrial players, second-sourcing for customers, and a diverse customer base. The main actors and their interdependencies in the generic foundry eco-system are shown in the schematic of Figure 6. Industrial suppliers are best positioned to accommodate the rapidly increasing demand and provide an agile response to evolving technology requirements. The suppliers form a complex inter-dependent eco-system with foundries, designers, original equipment manufacturers, design tool suppliers, and developers of intellectual property.
The key stakeholders will be addressed per domain in this chapter. Due to the complexity of the eco-system, we additionally anticipate a role for public subsidy to maintain open-access for new entrants. Here, the new European initiatives for Digital Innovation Hubs may provide a suitable framework.

JePPIX has proved particularly successful in bringing together the key players in the field of InP and TriPleX based photonic integration and in providing continuity. It provides a focal point for innovators on both the supply and demand side of PIC technology.

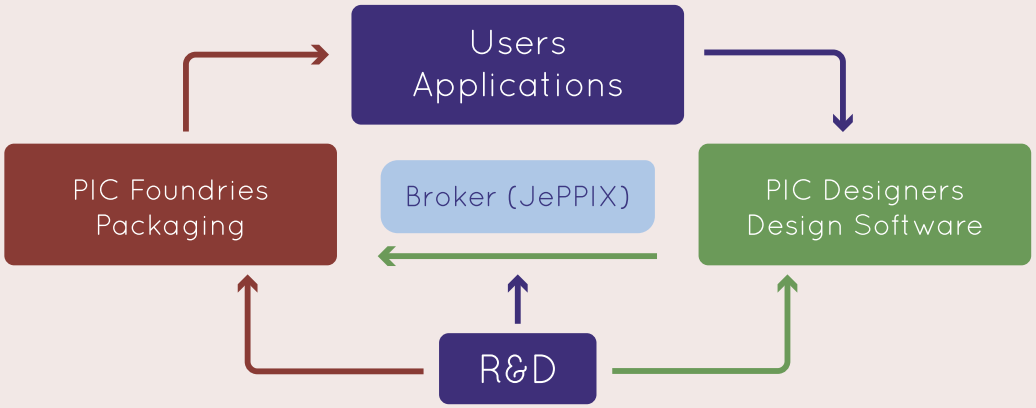

Figure 6 *The main actors and their interdependences in the generic foundry eco-system.*

The business case for PIC users

The largest group in terms of number of businesses and market size is the user base. Generic technologies enable the user to configure the circuit, creating diversity in design and an extensive range of markets. Considerable added value is created in the module for PIC-enabled products. The module can often have a value a factor of ten higher than the PIC itself due to the complexity of additional co-packaged components and the packaging technology. Many developers of PIC-enabled products have limited or no expertise in PIC technology, but are able to add considerable value at the module level. Many businesses have already started to explore PIC technology via JePPIX by prototyping on MPW runs. Hundreds of businesses are following the development of the field either through regular newsletter briefings or via the network of European Application Support Centers established by the PICs4All project to identify the best timing to adopt the technology. Early adopters are already seeing the benefits of mastering the use of PIC technology ahead of their competitors, but the learning curve has been steep while open access technologies have been in the early phases of development. As the technology matures and processes become qualified, future generations of products will benefit from accelerated product development cycles.

The business case for PIC designers and design tools

Professional PIC design houses like Bright Photonics and VLC Photonics have been a critical enabler for pioneer businesses and industry innovators. These businesses offer solutions for InP, SiP, SiN, and more besides to create a critical level of business, but specialization may be anticipated as the market takes off. Designers today have been skilled across many platforms and in some cases more than ten platforms, offering both a technology orientation service as well as key skills for creating viable designs ready for fab acceptance. The number of professional designers is increasing fast (but from a low base) as the number of businesses seeking to evaluate prototypes increases. This enables users and Original Equipment Manufacturers (OEMs) to access the technology quickly and with a lower risk, without skilling-up their own employees or recruiting from a relatively small talent pool. Close relationships are developing between professional designers and fabless/lableless SMEs, mid-sized businesses and corporations, guiding product development from early R&D phases to pilot production. The design house offers an attractive business model for skilled PhD graduates trained in the field as capital investments are currently relatively low. The operating costs are dominated primarily by software licenses and personnel costs.

Training programs such as those operated by JePPIX, and the wider access of university research groups to PIC technologies, will be instrumental to growing the talent pool and stimulating innovation. An emerging need for test services may also provide business opportunities for new professional services, and some design houses have also expanded their portfolio of services to testing.

Photonic design tools are numerous, addressing physical properties, interconnection, dynamics, layout, all the way through to system level prediction. Often even the choice of software package requires considerable skill to generate the relevant insight and viable design. Depending on the precise requirement, a complex combination of tools can also be needed motivating activity now in design automation. A number of JePPIX partners and software vendors address the challenge of developing circuit design tools with increasingly accurate building block representations and improved interconnectivity. A number of leading developers have joined the PDAflow initiative for photonic design automation with this objective in mind. A range of tool development opportunities are arising with a number of designers requiring a seamless environment for package, electronics and photonics. As technology matures, the accuracy of predictive design becomes a higher priority, and design for manufacture, showing the impact of manufacturing tolerance to the designer before tape out, becomes increasingly important. A significant number of software vendors already support process design kits provided by JePPIX foundries for increasingly accurate component and circuit level prediction. Standard templates for package and test are also becoming available for circuit layout tools.

The business case for foundries

The PIC foundries are the enablers of this rapidly evolving market. Forecasts are imprecise, but current indications are that the high PIC-enabled market penetration level (by value) observed for telecom transceiver technologies is likely to be replicated in a number of additional, larger market segments over the next five years. Data centre interconnects are the most immediate product-class which can benefit from high performance, low-energy products and open-access technology enables new entrants to develop PIC technologies for such markets. A robust generic foundry able to serve many markets does however require considerable up-front investment. The revenue becomes available only after the platform becomes sufficiently mature for the qualification of volume products. Precedents from the microelectronics sector shows that the foundry model is both profitable, sustainable, and enables a diverse and profitable industry around it in the longer term, but the starting phase can be several years. Fluctuations in load are an important factor in

the foundry business model, necessitating diversity in markets. We anticipate a continued mix of in-house manufacturers, integrated device manufacturers and pure-play foundries. A diverse range of customers enables dips in one market segment to be compensated by opportunities in others. The generic model is expected to give pure-play foundries an advantage in terms of accelerated design cycles for new entrants and new designs. In this sense, the open access foundry acts as a public good, enabling access to those outside the immediate industry. Nonetheless, the longer term sustainability of pure play foundries will also require a critical mass of volume products.

Packaging remains a barrier-to-entry to a number of users. Indeed, the packaging is often the starting point for a range of users who are otherwise technology-agnostic. The diversity in packaging specifications has so far fragmented demand, creating a barrier to entry for both suppliers and potential customers. JePPIX partners play a key role in defining package layout templates with a minimum set of standards to enable sufficient volume for tooling, processes and singulation such that the pricing for prototype packages approaches a viable level. JePPIX cooperates closely with the PIXAPP Packaging Pilot Line which is identifying business models and processes for volume scaling of standardised packages.

The business case for JePPIX as a broker

The eco-system requires both an orchestrator and an access point for customers who look for ease of access through a one-stop shop. A central organization is crucial for effective coordination of the whole eco-system, providing a supply chain to suit the needs for businesses and researchers starting out with PIC-enabled product development. JePPIX is playing such a role by addressing the following tasks:

- Combining designs from different users in Multi-Project Wafer (MPW) runs. The costs of R&D runs can be shared by many users, which leads to a dramatic reduction of the entry costs.
- Enabling the same processes to run independently of design. This decouples process-centering from product development, enabling a ramp up in time through technology readiness levels which is increasingly independent of any given product.
- Organizing documentation and training courses for the available foundry processes. Enabling ever increasing agreement between design tool predictions and fabricated chip performance.
- Reaching out to potential users and mentoring designers through the decision process and design-fab-package-test flow.
- Setting the strategic roadmap and providing leadership in this new technology sector.

JePPIX brokering operations empower the designer through web-based services, as well as technical orientation and training. As the number of businesses increases, and the products evolve, there will be opportunities for customers to configure value chains to their own needs, identifying the functions and services which best suit their own products. The services are currently focused on prototyping, but an increasing demand for product engineering and pre-production will require further scaling in support and documentation.

The brokering operation exists for the benefit of the eco-system and is not intended to be profit-making. In much the same way as for Europractice and MOSIS, there will be some reliance on subvention to maintain a skilled staff able to engage with new entrants and first users, while contributions to brokering costs from the suppliers will support activities for customers transitioning to small series production and pre-production.

4. Market Roadmap

The market potential is captured in terms of the high-growth predictions for markets leveraging photonic technology more generally, the recent breakthroughs for InP PIC technologies for telecommunications more specifically, and the uptake in the number of businesses using open-access technologies. We use a combination of published market data for custom InP PIC solutions and insights from JePPIX services to predict market penetration for the open access generic model.

InP-based PICs have become firmly established in the market place, with suppliers including Oclaro, Finisar, Lumentum, Infinera and Sumitomo shipping complex PIC-enabled products today. As shown in figure 7, besides other fields where PIC technology is becoming meaningful, InP PIC enabled transceivers already accounted for a 1 B€ market share in 2015 according to market research by LightCounting and the technology is predicted to

account for a 15% transceiver market share by value (5% by volume) in 2018. The breakthrough has been made with the roll-out of 100Gb/s per wavelength links, and the indications are that InP PIC market share will continue to increase with particular impact where performance is critical.

The roll-out of open-access generic integration technologies enables the technology to be exploited in new sectors. The most commonly acknowledged market sectors addressable by PIC technologies are summarized in terms of market growth in the figure on the next page. The front-runner market is transceiver technology, which currently receives considerable attention due to a pressing need from internet traffic growth and accelerated data center deployments. Medical segments such as optical coherence tomography (OCT) through to BioMEMs technology, also see considerable growth and are well positioned to adopt InP PICs and also TriPleX technologies. Fibre-optic sensing offers a considerable growth opportunity with drivers from the oil industry as well as structural engineering, industrial metrology and aerospace. Compound annual growth rates (CAGR) of order 10% to 20% are observed for photonic solutions in such markets. The increased need for free-space mapping and ranging is driving down the costs of LiDAR technologies, with likely impact in assisted driving, robotics, vision and virtual reality systems. These markets are anticipated to be further out in time, but the technology complexity required is motivating developments now.

For a broader market survey, the Market Research Study Photonics 2017 has been updated by the European Photonics21 public private partnership, breaking sectors out to production technology, measurement and machine vision, medical technology and life sciences, information technology, optical communications, flat panel displays, lighting, defense photonics, optical systems and components and photovoltaics. The global market for Photonics products in 2015 accounted for € 447 billion, growing at a compound annual growth rate of 6.2% from 2011-2015. While sectors such as flat panel displays, lighting and photovoltaics technologies have become commoditized, there remains considerable opportunity for innovation through photonic integration in the remaining sectors, all of which show solid growth.

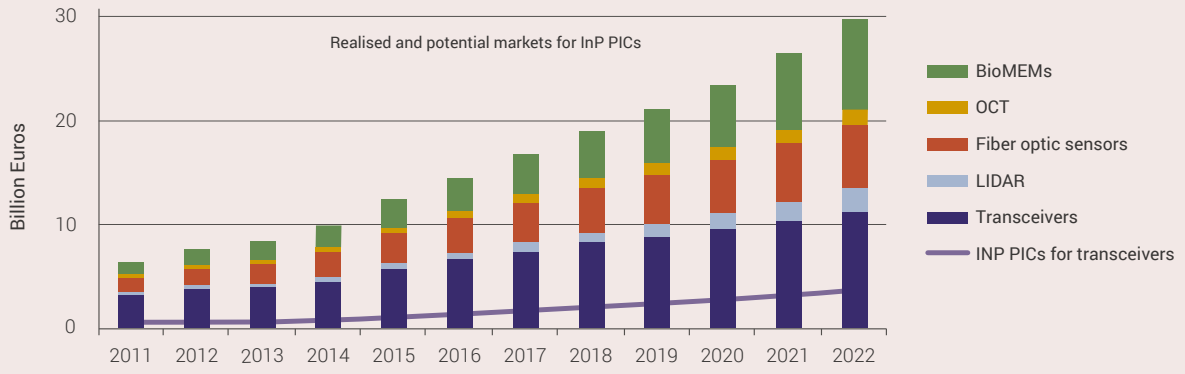

Figure 7 *Market growth for sectors where PIC technology is expected to have considerable impact. The line graph indicates the proportion of the transceiver market for InP PICs (realized until 2015 and anticipated to 2022).*[12345]

The ramp up in the numbers of designs is particularly important when evaluating the status of market development. The figure opposite shows the ramp up in terms of number of unique designs and also the origins of the designs.

The designs being voluntarily disclosed during the tape out cover a broad range of potential markets. (Note that designers are not required to disclose their domains of interest). A number of circuits can be classed as communications devices, from telecommunications and data-communications to microwave photonics and free space communications. Sensor interrogators have been designed for fibre optic sensors and free space sensing. Prototyping has also been performed for medical instrumentation, lab-on-chip diagnostics metrology and automotive devices through quantum optics.

1 Optical Coherence Tomography for Healthcare and Life Science: Technology and Market Trends, Tematys, September 2014 tematys.fr/Publications/en/oct/37-optical-coherence-tomography-for-healthcare-and-life-science-technology-and-market-trends.html

2 2015 Photonic Sensor Consortium Market Survey Report, Information Gatekeepers Inc, March 2015 igigroup.com/st/pages/photonic_sensor_report.html

3 BioMems: Microsystems for Healthcare applications, Yole May 2016, slideshare.net/Yole_Developpement/sample-bio-mems-2016-final

4 Market and Technology Briefing: Lidar Technologies and Applications, Yole, EPIC 2017 epic-assoc.com/market-technology

5 Integrated optical devices: Is Silicon photonics a disruptive technology? Lightcounting market research 2016 lightcounting.com/Silicon.cfm

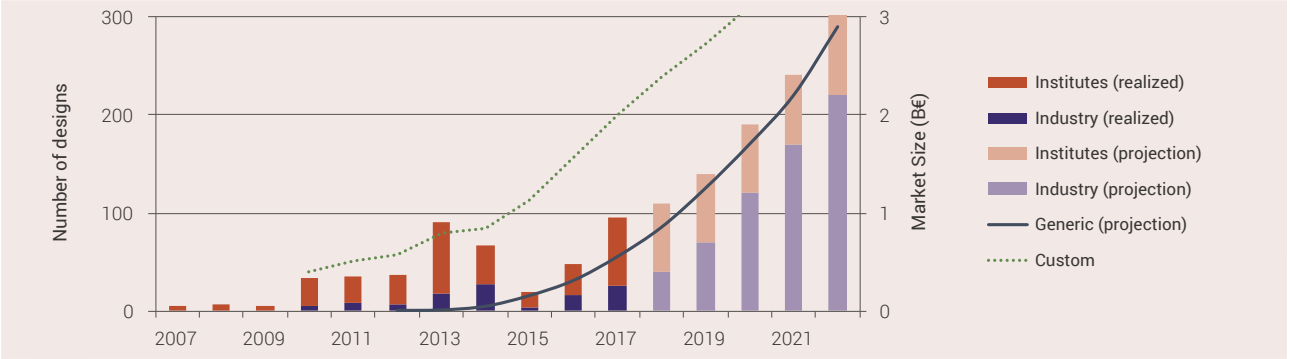

Figure 8 *Development of the application market enabled by ASPICs with projection of growth in volume to 2022. The bar chart shows the increase in JePPIX designs. The dashed line shows the market growth for custom InP transceiver PICs[5]. The solid line shows the market growth predictions made in the 2015 roadmap. Here a delay is foreseen because the prediction assumed a Manufacturing Pilot Line starting in 2016, which is delayed to 2019.*

JePPIX has now provided access for over ten years, transitioning from a purely academic activity to an industry dominated activity. The figure above shows a steady increase in tape-outs up to 2015. Here there is a drop-off at the end of two particularly important European projects (EuroPIC and PARADIGM), and a gap until a widely anticipated Pilot Line program. None-the-less, there has been a steadily increasing interest from businesses creating prototypes using the semi-commercial services.

In our earlier editions of the roadmap we specifically addressed the role of generic integrated technology and did not account for the role of incumbent platforms which were custom-product focused. This was considered to be a reasonable approach as the focus and value for generic technology is in enabling the accelerated adoption for PICs in new markets. Market size projections from the 2013 and 2015 roadmaps still provide a valuable guide to how the market may be expected to evolve. The first movers for PIC technologies have been companies with in-house PIC technology and they have been able to focus technology developments on the fast growing communication markets, leading to multi-billion Euro revenues a couple of years ahead of the forecasts for generic platforms. We now anticipate an acceleration in uptake with the European Pilot Line initiative planned for 2019. The diversity of emerging designs across multiple dynamic market sectors gives considerable confidence for a take-off in the not too-distant future. We see increasing activity for industry designers repeating and fine-tuning designs as they transition from an exploratory phase to a product qualification trajectory.

5. Technology Roadmap

As a result of significant investments in the development of foundry technology infrastructure, Europe has made substantial progress in this new way of working. The standardized open-access technologies that are provided by the two InP foundries SMART Photonics, Fraunhofer HHI and the SiN foundry LioniX International underwent steady improvements over the past years and have increased their range of offering. In this section we give an overview of the present status of the foundry capabilities, indicate where the technology goals from the previous roadmap were met and make a prediction for the status in 2020 and 2022. The predictions also take into account the results from a survey (presented in detail in Annex 2) that was filled out by more than 50 expert PIC users about their specific technology needs.

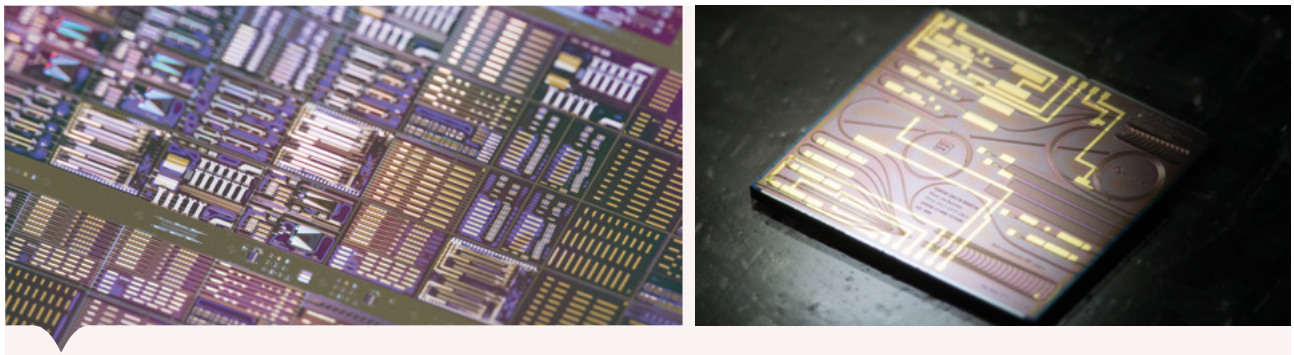

Figure 9 *Panoramic view of a processed InP multi-project wafer (left) and a PIC after chip singulation (right). Image by F. Lemaitre.*

Present Situation and Integration Trends

Presently, all three foundry partners offer commercial or semi-commercial access to their foundry processes through PDKs and have multiple MPWs per year each. Fraunhofer HHI and SMART Photonics both provide a full range of active and passive components, including lasers, detectors, modulators and passive elements, monolithically integrated on InP substrate. The TriPleX platform offers very low-loss passive components in combination with thermo-optic and piezo-electric elements and is well suited for hybrid integration with InP active components to form high performance lasers and interferometers. Different approaches for platform co-integration are being pursued, such as heterogeneous and hybrid approaches. These co-integrated future nodes are briefly discussed at the end of the section.

Present Capabilities

When comparing the present capabilities of the platforms with the predictions from the last roadmap release, we observe significant progress: most of the targets have been met. The list of building blocks available is shown in Table 2. In the following, we present the current technical capabilities of the generic platforms.

The Fraunhofer HHI platform supports very high-speed photodetectors, spot-size converters (SSCs), thermo-optic phase modulators and a variety of passive waveguide components. Recently transmitter components have been added: gain elements/SOAs, DFB lasers, DBR lasers, tunable gratings, EAMs and current-injection phase modulators. Furthermore, polarization splitters and converters to enable on-chip polarization handling are available. The RF detectors exhibit an internal responsivity of 0.9 A/W, a mean dark current of around 1 nA, and an electro-optical bandwidth of 40 GHz. SSCs provide 1.5 dB coupling loss to a cleaved Standard Single Mode Fibre. Waveguide propagation loss varies between <1 dB/cm for low-contrast waveguides to 2 dB/cm for high-contrast waveguides. MMI couplers and AWG de/multiplexers have typical excess losses of 0.5-1 dB and 2-3 dB, respectively. The current-injection phase modulators show 5 mA half-wave current values. The EAMs are characterized by > 20 dB static extinction and > 20 GHz bandwidth. DFB lasers exhibit threshold currents of around 10 mA and optical output power of > 20 mW (@100 mA) in integrated configuration with modulation bandwidth approaching 20 GHz at 100 mA bias current. SOA elements provide around 90 cm^{-1} gain and saturation power of 2 mW per 100µm device length. Insertion loss of the polarization rotator devices is ~1 dB with > 20 dB extinction. The platform is built on semi-insulating substrates to provide full electrical isolation of all the functional elements, and offers MPW runs on 3-inch wafers.

The SMART Photonics platform offers optical amplifiers, RF modulators, detectors and a variety of passive components. The SOAs provide up to 70 cm^{-1} gain and more than 20 mW saturation power. The phase modulators have been enhanced to support 20 GBd with 8 Vmm efficiency. More compact electro-absorption modulators operating with >20 GBd have been added as well. Detectors have > 0.85 A/W responsivity and 30 GHz bandwidth. Waveguide propagation losses are 2 dB/cm. Tunable DBR gratings with 50 cm^{-1} coupling coefficient are available for laser designs. In addition, ArF-scanner lithography has been introduced to the MPWs, which supports significantly improved performance for devices which require high resolution (e.g. AWGs) and high uniformity and reproducibility (e.g. interferometers). The platform has moved from 2" to 3" wafer size to improve capacity and uniformity.

The introduction of DUV lithography combines high resolution (<100 nm) with the possibility for volume production. It enables 20 nm critical dimension variation of the lithography which enables improved waveguide phase control. DBR gratings, for example, (Figure 10) have been demonstrated, as well as AWGs with waveguide gaps of 100 nm (Figure 11) which reduces the loss significantly. AWG central channel insertion losses close to 0.5 dB have been measured with a cross talk level lower than -25dB for all channels.

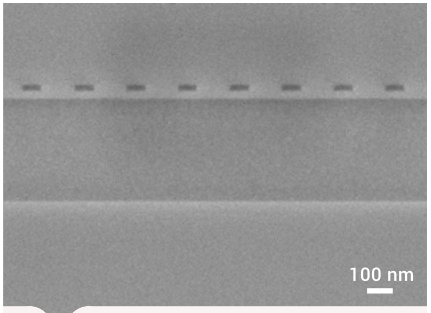

Figure 10 *Scanning electron microscope photograph of buried gratings for DBR lasers, fabricated with DUV lithography*[1].

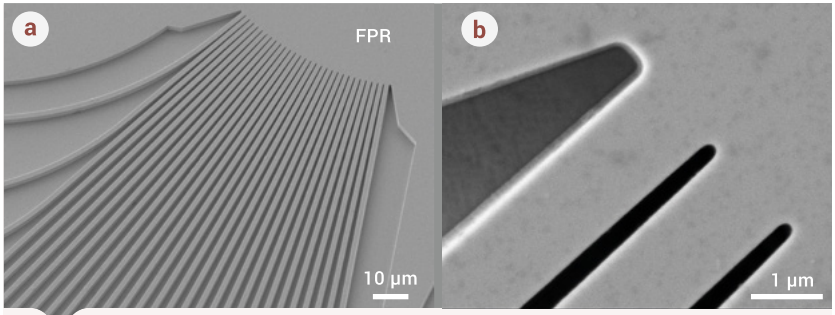

Figure 11 ***a*** *SEM photograph of an AWG at the junction with the Free Propagation Region (FPR).*
b *Zoomed in on the inter-waveguide gap.*
Image by J. Bolk.

The TriPleX platform offers low-loss straight waveguides, bends, S-bends, offsets, splitters, spot size converters, lateral tapers and thermo-optic phase shifters. Combinations of these building blocks allow, for example, the creation of microwave photonics ASPICs through combinations of Mach-Zehnder interferometers and micro ring resonators. The current platform has guaranteed losses below 0.5 dB/cm and results reported by customers have been as low as 0.1 dB/cm for the high confinement waveguides. Currently the PDK for visible light is under development in the PIX4Life pilot line project and it will be open to commercial users in 2018.

1 L.M. Augustin, "InP-Based Generic Foundry Platform for Photonic Integrated Circuits", IEEE Journal of Selected Topics in Quantum Electronics, 24(1), 2017.

Component	Target specification	Fraunhofer HHI	SMART Photonics
Lasers and Amplifiers			
SOA	Gain	92 cm^{-1}@7000A/cm^2	70 cm^{-1} @ 9000 A/cm^2
	Saturation Power	>3dBm	13dBm
DBR grating	Tuning range	4 nm	*
DFB laser	Tuning range	4 nm	*
	Output power	3 mW @ 150 mA	
DBR laser	Tuning range	4 nm	*
	Output power	3.5 mW @ 150 mA	10mW @ 100mA
Isolation section		yes	yes
Modulators			
Thermo-optic phase modulator	Loss	2 dB/cm	*
	I_π x L	20 mA x mm	
Current injection phase modulator	Loss	2dB for 100-200 µm	<0.5 dB for 2 mm
	I_π x L	20 mA x mm	t.b.d.
Electro-Optical phase modulator	Loss	*	<0.5 dB for 2 mm
	Bandwidth		8 GHz
	U_π x L		8 V x mm
PIN photodiode			
	3 dB bandwidth	>35 GHz	>30 GHz
	Dark current	10 nA @ -2 dV	<25 nA @ -2 V
	Responsivity	0.8 A/W	>0.85 A/W
Passive components			
Straight Waveguide	Loss	<2 dB/cm	2 dB/cm
Arc waveguide	Minimal radius	150 µm	100 µm
Spot size converter	Loss	2 dB to cleaved SSMF	*
1x2 MMI coupler	Loss	<1 dB	<1 dB
2x2 MMI coupler	Loss	<1 dB	<1 dB
1x2 MMI reflector	Loss	*	1.5 dB
	Reflectivity		35%
1x1 MMI reflector	Loss	*	1 dB
	Reflectivity		80%
Polarization splitter	Loss	<4 dB	*
	Polarization extinction ratio	>25 dB	
Polarization converter	Loss	<3 dB	*
	Extinction	>10 dB	

Table 2 *List of building blocks offered at the close of 2017 for the InP MPW runs.*
** Building blocks under development.*

Component	Quantity	Specification
Passive waveguides		
Straight waveguide	Propagation Loss	0.5 dB/cm
Arc waveguide	Propagation Loss	0.5 dB/cm
Tapered waveguide	Loss	0.5 dB/cm
S-bend waveguide	Loss	0.5 dB/cm
Connectors	Loss	0.5 dB/cm
Passive components		
Spot size converter	$1/e^2$ Mode Field Diameter	10 µm
Y junction	Loss	0.5 dB
Directional coupler	Loss	0.5 dB
Modulators		
Phase modulator	Loss $P_{2\pi}$	0.5 dB/cm 500 mW
Phase modulator (arc-type)	Loss $P_{2\pi}$	0.5 dB/cm 500 mW
Electrical elements		
DC pad	Width	100 µm
DC bond pad	Size	500 µm
Heaters	Radius	100 µm
T junction	Size	500 µm

Table 3 *List of building blocks offered at the close of 2017 for the TriPleX MPW runs.*

Roadmap 2020

In 2020 the SMART Photonics and Fraunhofer HHI platforms plan to offer an extended library of components and provide statistical data of building blocks and wafer verification data.

The Fraunhofer HHI platform will provide increased performance and reproducibility. In 2020 it will be capable of supporting a Tx/Rx symbol rate of 56 GBd on the Tx side accomplished by electro-absorption modulators. Tunable lasers with wider tuning range and lower linewidth will be introduced and advanced polarization handling devices will be available for implementing polarization-multiplexing and polarization diversity functionalities. Out-of-plane coupling mirrors (45°) will be available allowing for automated on-wafer measurement of PICs. Aluminium-based active devices will be added to the platform for more robust performance at high temperature. All building blocks will have statistical performance data.

The SMART Photonics platform will provide more functionality by adding spot-size converters (< 1dB loss) and high-speed RF

interconnects (> 60 GHz). Together with further bandwidth and efficiency improvements in the modulators and detectors, the platform will be well suited to address high-speed Tx/Rx applications. Both EAMs and MZMs will support 40 GBd operation with < 3 V drive voltage and < 5 Vmm efficiencies. Detectors will have 30 GHz bandwidth and balanced configurations will be supported. This is complemented with simple electrical passive elements such as resistors and capacitors. The option to choose some of the epitaxial material systems will be available as well.

The TriPleX platform will add more advanced building blocks to its current library and optimize the waveguide further to an even more robust waveguide cross section. This will be implemented as a PDK upgrade. Structures like AWGs and Micro Ring resonators are on the roadmap of LioniX for implementation in the platform. In addition the implementation of stress induced (PZT) tuning elements in the PDK is foreseen to enable low power tuning of the TriPleX waveguides. LioniX will also start offering the implementation of narrow linewidth light sources in their PDK by offering hybrid integration with InP including packaging. The guaranteed loss will be lowered close to the best-case reported value of 0.1 dB/cm.

Roadmap 2022

InP platforms will reduce their passive waveguide losses to < 1 dB/cm and have supporting building blocks for RF and DC interface connections.

The Fraunhofer HHI platform will be further enhanced with high-speed (56 GBd) Mach-Zehnder type modulators. Production will be transferred to 4″ PIC wafers, and spectrally C- and L-band will be accessible thanks to the introduction of dedicated wide-gain active material.

The SMART Photonics platform will offer different versions of its platform. Next to a state-of-the-art high performance platform for data and telecom applications, a low-cost platform will be supported to focus on high volume applications in emerging areas such as sensing, imaging and healthcare. The wavelength band around 1.3 µm will be part of the new platform offering.

The TriPleX platform will offer process design kits also for other wavelength ranges and further integration of hybrid InP combinations is foreseen.

Fraunhofer HHI	
Component	Expected performance
EAM (phosphorus based)	56 GBd transmission rate
EAM (aluminum based)	70 GBd transmission rate
EOPM (phosphorus based)	56 GBd transmission rate
Improved polarization devices	>20 dB extinction ratio
Out-of-plane coupling mirror	2 dB insertion loss

SMART Photonics	
Component	Expected performance
Spot-size converter	< 1 dB insertion loss
RF interconnects	> 60 GHz 3-dB bandwidth
Modulators (EAM and MZM)	56 GBd transmission rate
Photodetector	> 50 GHz 3-dB bandwidth
Electrical passive elements	

TriPleX	
Component	Expected performance
Arrayed-waveguide grating	ITU grid 8 and 16 channel
Micro rings	single ring on ITU grid
PZT tuning elements	2π phase shift at μW tuning power
Waveguides	0.1 dB/cm propagation loss

Table 4 *List of platform components expected to be added by 2020.*

Future Technology Nodes

As PIC technology development continues, novel schemes will emerge either to enable new applications by combining different technologies in a reliable way or to continue scaling the density of components for very large scale integrated (VLSI) photonic systems. Research lines are targeting new technology nodes within a period of five to ten years.

Hybrid InP-SiN integration

For both SiP and SiN, lasers and amplifiers have to be integrated in a hybrid way. By hybrid integration we understand an approach in which different chips are coupled after processing. Hybrid integration technology has made considerable progress. It is especially favourable where the PIC requires component properties which cannot be provided by a single platform, for example optical gain and very low loss. The integration of InP active components (lasers and modulators) is on the roadmap of LioniX International, and will be implemented in the TriPleX PDK and offered in MPW services.

	Performance		
Building Block	**InP**	**SiP**	**SiN**
Passive components	●●	●●	●●●
Polarisation components	●●	●●	
Lasers	●●●	H	H
Phase modulators	●●●	●●	●
Electro-absorbtion modulators	●●●	●●	
Switches	●●	●●	●
Optical amplifiers	●●●	H	H
Detectors	●●●	●●	H

Performance	
●●●	Very good
●●	Good
●	Modest

Fabrication Technology	
H	Hybrid/Heterogeneous

Table 5 *Performance comparison between three major platform technologies.*

From table 5 it is seen that InP and SiN are perfectly complementary. A successful hybrid platform integrating InP and SiN components will offer, therefore, superior performance for both active and passive components and is a very promising approach for complex PICs which require very low propagation losses, e.g. in delay lines or high-Q filters. Ultra-low linewidth lasers by combining InP and TriPleX chips from LioniX and Fraunhofer HHI have recently been reported[1]. The TriPleX platform will not only allow the combination of efficient InP lasers with ultra low-loss passive waveguides, but it will also enable testing of InP circuits on wafer scale by using TriPleX-based optical waveguide probes.

Heterogeneous InP-Si electronics

By heterogeneous integration we understand an approach in which an unprocessed or partially processed wafer or die e.g. InP, is bonded to a processed wafer, e.g. silicon photonics or CMOS, and further processed on wafer scale after bonding. Heterogeneous integration of InP lasers and amplifiers on SiP circuits offers more flexibility in placement of lasers and amplifiers than hybrid integration, at the cost of added complexity in the fabrication process, because processing of both InP and SiP circuitry is now required. Further, the coupling between the InP and the SiP layer introduces coupling losses of 1 dB or more, and the coupling structures require significant space, of in the order of 100 µm per coupler depending on the substrate design.

1 Integrated-photonics laser has record-narrow chip-based linewidth of 290 Hz
http://www.laserfocusworld.com/articles/2017/07/integrated-photonics-laser-has-record-narrow-chip-based-linewidth-of-290-hz.html

Heterogeneous integration of InP-Photonics on Silicon Electronics avoids optical coupling losses as only one PIC technology is used, and offers high-performance electrical connections. To this end, JePPIX partners are working with microelectronics partners on a so-called Photronics platform. The approach consists in adapting the generic InP photonic integration process such as to make it suitable for wafer scale bonding onto a (Bi)CMOS wafer in which the driver, receiver and control electronics are integrated. The bonding is achieved by means of a polymer layer that is optically and thermally insulating, and thermal, mechanical and electrical connections are made with vias through the bonding layer. New components such as passive RF elements will be available either on electronic, photonic or intermediate layers, and building blocks for broadband interconnections will help improve integration density and circuit functionality. The photonic-electronic co-design will increase device speed and reduce power consumption. These efforts are expected to result in combined photonic-electronic MPW services in the longer term.

InP membrane on Silicon

The InP membrane on Silicon (IMOS) platform aims at further reducing the footprint of photonic devices by moving towards a high contrast waveguide technology embedded in an InP membrane that can be fabricated on Silicon wafers. It has seen significant progress since the start of the technology and now offers a range of passive waveguide components such as MMIs, ring resonators, directional couplers, dielectric and metallic grating couplers, and polarization converters. Lasers realized with active-passive integration have also been demonstrated recently. First experimental MPW runs with amplifiers and passive building blocks will be carried out in 2018 on a research basis. In 2020, it is planned to launch an experimental nano-photonic platform which includes optical amplifiers, high speed uni-travelling-carrier detectors and polymer-based slot-waveguide modulators, alongside the suite of existing active and passive building blocks.

6. Process Design Kit and Library Roadmap

Allowing designers to create a mask layout that can be submitted to a JePPIX foundry is one of the key elements of scalability of the generic integration technology. The introduction of Process Design Kits (PDK) back in 2008 together with the Multi Project Wafer (MPW) runs has largely supported the transition of PIC technology from academic research into commercial manufacturing. The potential of a foundry process is, to a large extent, determined by the maturity of the technology, reflected in the contents of the PDK. Such a PDK needs to be compatible with design software from several vendors and contains in general:

- Process information, describing a simple view of the mask layers involved in the fabrication process.
- Pre-defined mask layouts, specifications and models for a set of Basic Building Blocks (BBB).
- Mask layouts and models for a variety of more complex Composite Building Blocks (CBB) that can be grouped to form component libraries.
- A set of Design and Verification Rules

The set of Basic Building Blocks are enabled by the process technology as described in chapter 5 and their specifications are guaranteed by the foundry. A variety of CBBs can be created out of the BBBs, enriching the PDK content of the foundries, facilitating the design of application specific photonic circuits (ASPIC) and also forming proprietary component libraries. Both the set of BBBs and the component library that groups CBBs can be extended to hold simulation data in form of compact or physical models, which is in turn provided to simulation software tools.

Present Situation

Each of the three JePPIX foundries have a process design kit containing a component library of Basic Building Blocks and the most commonly used Composite Building Blocks. Since the 2015 roadmap release, more content has been added to the PDKs. Both InP foundries have included mask layouts and specifications for the newly developed technology components from chapter 5 such as transmitter (SOAs, lasers) and polarization handling blocks in the case of HHI and EAMs, gratings and detector building blocks in the case of SMART Photonics. LioniX is actively extending its PDK, adding more Composite Building Blocks for tele and datacom wavelengths and a version for visible light applications. An overview of the available library components is given in Table 6.

	SMART PDK	HHI PDK	Lionix PDK
BBB	WGs with 2 index contrasts	WGs with 3 index contrasts	Straight, arc, taper bend
	Straight, arc, taper bend	Straight, arc, taper bend	Spot size converter
	Photodetector	Spot size converter	Phase modulator
	RF Photodetector	Waveguide transitions	Y-splitter
	Semiconductor optical amplifier	MMI couplers	Directional coupler
	Mode filter	Photodetector variants	
	DBR grating	Polarization components	
	Electro-absorption section	Thermo-optic phase modulator	
	MMI reflectors	Current-injection phase modulator	
	MMI couplers	Semiconductor optical amplifier	
	Waveguide transitions	DFB laser	
	Electro-optic phase modulator	AWG	
	AWG		
CBB	Electro-absorption modulator	Electro-absorption modulator	Mach-Zehnder interferometer
	Mach-Zehnder modulator	DBR laser	Optical beamformer
Misc	DC pad	DC pad	DC pad
	RF pad	RF pad	
	RF CPW track	RF CPW track	
	Waveguide crossing	WG-metal crossing	
	Electrical isolation	Electrical isolation	
		Impedance matching RC	

Table 6 *Components offered in foundry PDKs.*

Third-parties are engaged in creating more complex CBBs and grouping them into component libraries that complement the basic offering of the foundry PDKs. Custom passive components such as advanced AWGs, MMIs or active components such as widely tunable lasers and high-speed modulator modules from research institutions and design houses are being incorporated into these libraries, enabling more functionality and a speed up in the design process for end users. A standard framework to enable easy extension of the existing PDKs exists and is being improved to speed up the development of library components. In addition, generic

packaging templates and standards have been integrated and made available for the main packaging partners through collaborations in European projects such as through the PIXAPP project.

The design manuals for the generic foundry processes contain the performance parameters of most of the offered components but the specifications are not fully complete yet. Furthermore, the effects of statistical variations need to be reflected in the specifications. To have complete and reliable statistical data, automated building block characterization and performance tracking will become standard procedures.

Standardized Interface

The concept of the component library that can be filled by third-parties with advanced CBBs is of high importance for the generic foundry model and has the prospect of becoming a business of its own as is the case in the electronic integration industry. Presently, not many CBBs are easily available to all users as they are developed in different tools. To maintain a continuous growth of library content, assuring compatibility of the PDK with design and simulation tools from different vendors is crucial. Therefore a common framework is necessary in which design software can interface with foundry PDKs and communicate with each other. The PDAFlow API, as developed within EU-funded projects and now managed by the PDAFlow Foundation, has taken a central role in providing such a common framework, which is described in the next chapter in more detail. With the increase in the number of components and tool providers, it has to be extended to incorporate the interfacing with simulation models and the support of a licensing model for IP building blocks. To address these aspects work on an open PDK standard with an efficient version control and governance structure is required. Furthermore, convergence of this PDK standard with its electronic counterpart to facilitate the trend towards integration of photonics with electronics is necessary and will be worked on.

Roadmap 2020

The process design kit will contain statistical data on mean values and 3 sigma control limits for each BBB, determined from a series of fabrication runs by automatically measuring in-line and off-line test structures. Calibration data for simple compact models will be incorporated into the PDK that relate design variation and fabrication tolerances to device performance and that are seamlessly integrated with simulation tools through a common data exchange standard.

More advanced CBBs will be developed and made available for different application sectors, e.g. for communications, microwave photonics and optical sensing. IQ vector modulators and coherent receivers operating at 25 Gb/s together with tunable lasers < 300 kHz linewidth will be offered with < 1 pJ/bit transmit power efficiency. Widely tunable laser modules with > 40 nm tuning and > 3mW output power and pulsed lasers with adjustable repetition rate up to 30 GHz will be available. High speed receivers (50 GHz) with saturation input powers up to 10 mW will be part of the offering. The open PDK framework will be accepted as a standard and additional CBBs originating from the pool of ASPIC designs from the eco-system will complement the library offer.

In addition, generic test templates will be added to the libraries, facilitating optical and electrical testing and packaging. This involves templates for DC and RF pad placement but also schemes for edge and vertical fibre-to-chip coupling to assist standardized packaging and on-wafer testing.

Roadmap 2022

The amount of available statistical performance data will be extended to the component library and its CBBs with compact models describing their behaviour. Seamless integration of the PDK into the design workflow with a standardized PDK structure and data transfer formats will be implemented and maintained in an open environment. This will allow accurate and fast modelling of passives and actives in circuit simulation tools, with calibrated compact models. In addition, test procedures can be defined during the chip design phase and performed virtually in design and simulation tools.

Initial interfaces to electronic PDKs will be established to enable the co-design of electronic and photonic circuits. Modulator and detector CBBs will have corresponding driver and receiver building blocks in the respective electronic PDKs with simple co-simulation models attached. In addition, interconnection building blocks and passive RF components will be provided to support the heterogeneous integration technology.

7. Photonic IC Design Tools and Flows Roadmap

PDKs and Layout

As described in chapter 6, the introduction of PDKs and MPWs has fuelled innovation in the domain of integrated photonics technology. The effective sharing of key information within the design community enabled engineers with little understanding of the actual fabrication technology to make designs that deliver the required functionality and are actually manufacturable. As mentioned before, the description of mask layouts for various basic and composite building blocks allowed designers to pick, place and connect blocks to create functions for a specific application. To allow for customized design within the boundary conditions of a particular process, the PDK needs to hold information that can help designers to validate the manufacturability of their designs. Adding these so called design rules to photonic PDKs is now also common practice in the electronics industry.

Design Rule Checking

Design rule checking needs to be implemented on two levels. First, the mask layout software implements design intent checking, by ensuring that parameters are within the range as specified in the Design Manual and that basic rules for good circuit design are followed. Some of these are presently in place and give an early warning to designers if rules are not followed. Secondly, the resulting GDSII mask files themselves are submitted to Design Rule Check (DRC). This will mostly flag violations of (technology) rules set by the foundries. A number of such DRCs are presently in place for the JePPIX foundries. A much more extensive set of such DRCs is being developed, and checking should be an automated service performed by software tools, since manual checking is labour-intensive and error-prone.

Component Modelling

Models for both frequency domain as well as time-domain circuit simulation are becoming available, to enable a full design flow from circuit design to verified layout. To further develop the automation of designing photonic integrated circuits and systems, tools and flows activities are ongoing at several software vendors, design houses and academia, supporting PDK driven as well as custom design within the boundaries of the generic fabrication technology.

Depending on the end-application and complexity of the design (e.g. the number of components, or the balance between photonic and electronic components) the most applicable tools or flow might be different. The picture below depicts the different abstraction levels in the full design flow and is used to illustrate the development focus points for the coming years.

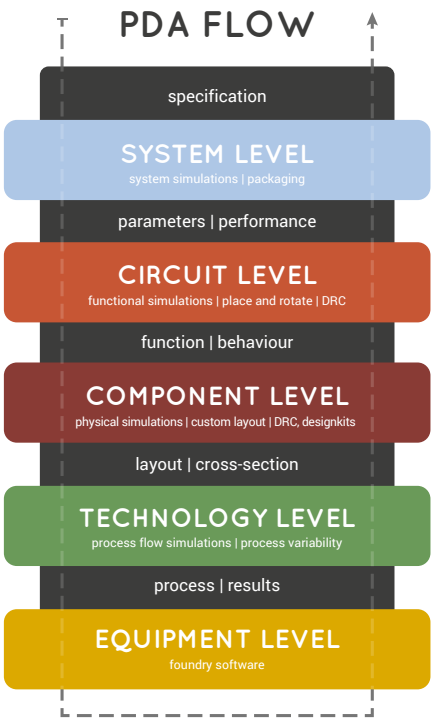

Figure 12 *Overview of abstraction levels in the PIC design flow.*

Present situation 2018

Component-level simulations are in general well-developed. For the photonic performance of passive devices there is a rich choice of (commercial) tools that provide accurate (physical) simulation results. Various numerical methods can be tailored to the specific problems. For simulation of devices which require (time-domain) modeling of the electro-optical interactions, there are fewer tools available. Proper simulation requires more in-depth knowledge about the device operation, in order to judge which approximations can be justified. Dedicated software exists for the simulation of (integrated) laser diodes based on physical parameters. Time-domain device simulations of active components which are available from the foundry PDK library are now starting to appear, but the choice is still limited. Such simulations should be based on device parameters that have been extracted from the PDK library components. Simulation of the (RF) dynamic performance of electro-optical devices is very limited and co-simulation which includes the (RF) electronic driver circuit as well as the component environment (package) is presently not available at all. The world's major vendors of Photonic Design Automation (PDA) solutions have become members of the PDAFlow Foundation to collaborate on tool interoperability and PDK standardization.

Roadmap 2020

To address the increasing complexity of the photonic circuits design tools will have to be able to automate more designer tasks at circuit level. In the Electronics Design Automation space, the most common flow is called Schematic Driven Layout (SDL). The first step is to capture the designers' intent at circuit level, perform simulation for the whole

circuit and when satisfied move to the layout phase. The PIC industry seems to be ready to move towards such a working model, but is held back by a lack of compact models for the components in a PDK. The priority should be to provide the circuit capture capability, with simplified generic models, to start supporting a SDL flow, meanwhile improving the models to become more and more accurate when simulating the (full) circuit. To design more robust circuits for a wider operating range, adding more modelling capabilities, particularly thermal models, is required. The next step is to move from a simple netlist exchange obtained from the circuit tool to a layout environment, and then to a full bi-directional interface between schematic and layout, to make sure that changes made at layout level are back-annotated to the intended circuit and can be re-evaluated.

In addition to the improvements in the circuit design environment, more automation is required for the layout phase. When complexity goes up, more placement of components is needed and more interconnections need to be made. In electronics this is called Place and Route, and it is a significant step in the whole design process. For digital IC design it is most completely automated, for photonics there is emerging automation. We expect to see more auto layout generation from schematics, more auto-routing of waveguide connections and more automated DRC capabilities. Commercial tools exist to perform this automated design rule checking, but the PDKs need to become more mature by adding more design rules to the DRC deck. Finally, it should be possible to perform Layout versus Schematic (LVS) checks by taking a final mask layout design and reconstructing the intended circuit. This is a very important step to ensure that the final design is and manufacturable (after DRC) and compliant with the designers' intent. Current electronics tools are not able to perform LVS on photonics designs, as the concept of "open" and "short" for electrical wires is not applicable for optical waveguides.

For more integrated design flows and richer PDKs, collaboration is a key enabler. The PDAFlow Foundation, created in 2013 by JePPIX partners Filarete, Photon Design and PhoeniX Software and extended by JePPIX partners VPIphotonics, TU/e and Bright Photonics is developing and maintaining standards and interfaces for defining photonic PDKs that are compatible with software tools from multiple vendors and an API supporting tool interoperability. Besides these developments in the PDAFlow foundation with almost ten members today, other bilateral collaborations between a variety of software vendors exists to develop electronic-photonics design environments and/or interface layout and simulation tools. We expect that these activities will further intensify, helping the industry to make more complex designs with a higher quality in less time. Another trend is the development of open-source models to stimulate open innovation and further promote open access MPWs.

Roadmap 2022

Further automating the design flow will require more enhanced simulation routines combining time-domain, frequency domain, co-simulation of electronics and photonics and finally also including crosstalk, scattering and other parasitic effects. However, the main focus will be on adding full process variations aware simulation capabilities throughout the whole design flow. This requires fabs to add this information into their PDKs, and the software tools developed to use this information to perform full yield analysis.

In addition, the need for design for packaging is becoming more prominent. This includes for instance the ability to simulate (RF) signals to and from the chip throughout the package to a printed circuit board or an electrical die in the same package. Further, optical, mechanical and thermal modelling of a sub-system or complete system are required to develop more complex systems making use of photonic ICs.

8. Packaging and Testing Roadmap

Delivery of packaging solutions must address the twin requirements of a convenient, low-cost prototyping solution at the start of the design cycle, and the seamless migration to a larger volume, lower-cost module suited to system integration. Whereas small-to-medium volumes call for generic packaging solutions for obvious cost reasons, high volume products tend to use specifically adapted packages to achieve optimum size, best performance, and/or cost savings.

The progress in generic photonic integration platforms is generating a rapid increase in demand for PIC packages. The users differ in size, ranging from start-ups and small to medium enterprises (SMEs) to international corporations, and intended uses vary widely. These factors have a direct impact on the expected volumes and target costs per module.

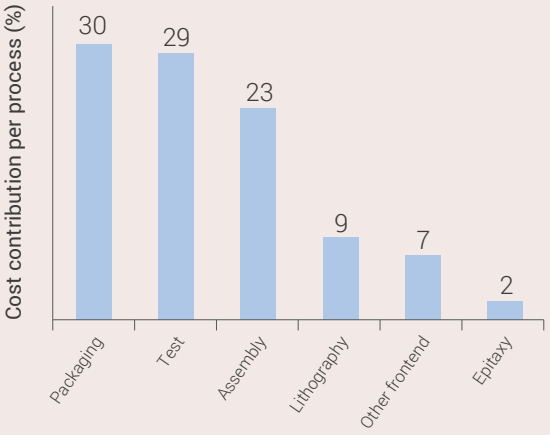

Figure 13 *The contriburion of manufacturing processes to the overall cost of monolithically integrated devices.*[1]

In order to keep PIC based solutions feasible and economically viable the technology processes have to be highly reliable to assure maximum yield and scalability to keep-up with increasing volume demands. One of the major bottlenecks, and at the same time significant contributor to the overall final PIC product costs, is related to testing, assembly and packaging across the full supply chain, as presented in Figure 13. Although the data in the plot is based on a study dating from some 12 years ago the challenges remain valid today and clearly indicate that R&D efforts are to be increased in these areas in order to increase accessibility to PIC technologies and meet economical targets.

8.1 Packaging

Low-barrier-to-entry PIC package solutions are addressed by JePPIX partners Technobis, LioniX, Cordon and Tyndall. A route to small and medium volume production of packaged PICs is being developed in the framework of the PIXAPP packaging Pilot Line coordinated by Tyndall. In the following section, solutions available as of 2018 from JePPIX partners will be presented with their typical features listed. Expected evolution of those offerings along with an impact assessment of current assembly and packaging technology developments will be discussed in the following paragraphs over a four year timescale.

2018

Whilst developing a photonic system, typically a proof of concept is required first. Here the overall package dimensions are of less importance. Photonic packaging, using a customized package design, may be relatively expensive for both PIC prototyping and small series production, as non-recurring engineering (NRE) costs will dominate over the bill of materials. In order to enable testing first versions of PICs at reasonable entry cost some standard packages are currently available as presented in Figure 14.

1 Erica R. H. Fuchs in IEEE JLT, vol. 24, No.8, 2006.

These generic packages provide a restricted range of features such as the maximum RF bandwidth, the maximum amount of electrical connections, and a limited number of chip sizes supported. Typically, the configuration of the PIC has to follow electrical and optical I/O layout rules to comply with assembly design rules. They are useful in a wide range of applications for many users but may not represent the ultimate solution for real products. Such generic packaging solutions are mainly intended for lab-bench characterization and advanced prototyping, and typical parameters are listed in Table 7.

	Technobis	CORDON/Linkra	LioniX International	PARADIGM/Tyndall
Package type	G5 generic test package	52 pin package	Full characterization package	PICOSA
DC ports (max)	91 (3 sides)	48 (2x24)	80 (2x40)	min. 36 (3 sides)
RF ports (max)	4 (1GHz typical, up to 10 GHz max)	4 (40GHz)	NA	4 (10Gb/s)
Optical ports (max)	1	32	64 (2x32)	4
Fibre array option	Yes	Yes	Yes	Yes
TEC/Thermistor	Yes	Yes	heat sink only	Yes
Die size (max)	6 mm x 6 mm	10 mm x 10 mm	16x16 mm ; 8x32 mm	9.5 mm^2
Lead time	1.5 months	3 months	1 month	+6 months
Design Rules	Yes	Yes	Yes	No
Design Kit	Yes	Yes	Yes	No
Unit price (min)	995 €	2,000 € - 3,000 €	1,500 -4,000€	2,000 €+
Standardized PIC layout	Own standard	Own standard	Yes	Own standard
MPP runs	Yes	No	No	No
PIC platform	InP, SOI, TriPleX	InP, SOI, TriPleX	TriPleX	InP
Automated Pre-package test	No	No	No	No

Table 7 *Low-barrier-to-entry prototype package solutions available on the market in 2018.*

Technobis has developed a generic package shown in Figure 14(a). This packaging process suits the PIC development and testing phase and is also offered on basis of Multi-Project Packaging (MPP) runs. Assembly design rules are available to PIC designers and implemented in the PIC design tools.

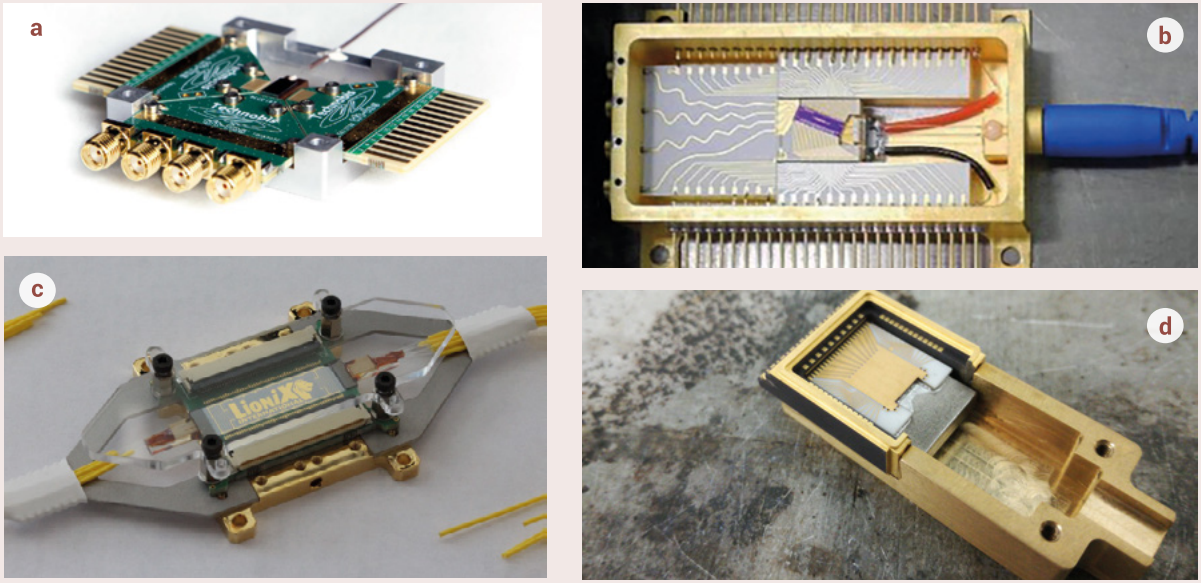

Figure 14 *Generic prototyping packages for lab bench evaluation and advanced prototyping.*
a *Generic Test Package from Technobis BV.*
b *Standard 52 pin InP ASPIC package from Cordon Electronics.*
c *Full characterization package for TriPleX based ASPICs from LioniX International.*
d *Generic package designed in the EU funded PARADIGM project, and currently further developed at Tyndall National Institute.*

Technobis is currently expanding its packaging and assembly facilities towards a volume packaging infrastructure and expects to offer such services to external customers by the end of 2018. Cordon Electronics (previously Linkra) continues to support the generic packaging solution developed at Linkra for JePPIX MPW users. The generic package presented in Figure 14(b) is a standard catalogue item, although lead-times could slightly vary depending on the workload and number of samples to realize. A set of packaging design guidelines and templates is offered to PIC designers to aid the process. The assembly design rules are implemented in mask design software packages. LioniX International offers a characterization package, as presented in Figure 14(c). This package comes with the corresponding design rules and is offered as a standard solution to TriPleX MPW participants. Tyndall National Institute is developing a more capable generic package, which was initiated in the EU-PARADIGM project, Figure 14(d).

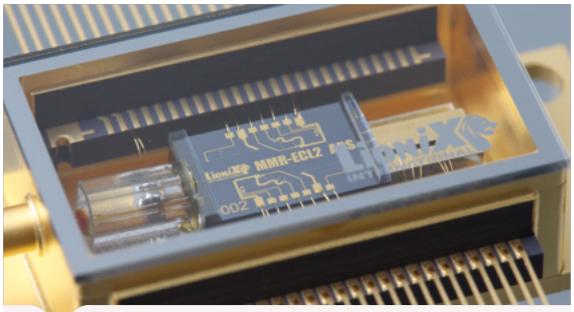

Figure 15 *Hybridly integrated (InP and TriPleX) low linewidth laser from LioniX International.*

There are current developments at LioniX International to hybridly integrate InP and TriPleX PIC chips in a single package as presented in Figure 15. Industrialization of those processes is expected to be launched in volume during this year using the recently started assembly foundry PHIX.

2020

Today's low-entry-cost (Table 7) generic packaging options are based on customized builds which are internally standardized (at a company level) at most and suffer from lack of automated assembly and scalability. Highly automated and scalable processes are crucial for moving from a prototyping phase to mid or large volume manufacture. To enable the anticipated uptake in open access technology, standardization in test protocols and assembly and packaging technology processes will become increasingly important. This trend will also have an economic impact on providers of assembly equipment, in that the high research and development costs associated with individual request for automated systems can be reduced.

In recognition of the existing packaging issues in photonics the European Commission is supporting a joint effort in setting up the first global scale open access photonic integrated circuits packaging and assembly pilot line (PIXAPP). JePPIX is providing inputs to the development and validation of assembly and packaging processes for InP PICs and contributes to other photonic integration platforms. Developed solutions will be demonstrated in four different application domains (Table 8), with modules targeting bio-sensing, fibre sensing, tele- and data communications; all of which pose specific challenges not only to packaging and technology solutions but also to acceptable costs and expected lifetime (Table 9).

	2018	2020	2022
Price per unit	2000 €	<2000 €	<500 €
Lead time	3-6months	two weeks	<two weeks
Assembly processes implemented	Mainly customized	Unified processes	Standardized processes
Level of automation	Low	semi-automated	automated

Table 8 *Roadmap for generic package solution for ASPICs.*

Application	DataCom	TeleCom	BioSensor	Fibre Sensor
Envisaged lifetime	3-5 years	25 years	single use	>25 years
Cost per unit (EUR)	hundreds	hundreds	few	thousands

Table 9 *Four demonstrators for different application domains under development in the European PIXAPP pilot line.*

Standardisation is critical to enabling a seamless transition to manufacturing and volume production. JePPIX and PIXAPP are defining standardised PIC templates for MPW dies: as an example features of a template for InP PICs from SMART Photonics MPWs are listed in Table 10. This will enable a generic test service. Via such a service, fabricated dies can be characterized automatically following user predefined test scripts (measurement description file).

	JePPIX-PIXAPP
Package type	Generic (from 2022)
DC ports (max)	114 (north and south)
RF ports (max)	4 (GSG)
Optical ports	25µm grid
Fibre array option	Yes
Design Rules	Yes
Design Kit	PhoeniX/Nazca/Luceda
Standardized PIC layout	Yes/JePPIX-PIXAPP
PIC technology	InP
Automated Pre-package test	Yes

Table 10 *Features of the standard template for test and packaging developed by JePPIX – PIXAPP for chips from SMART Photonics MPW services.*

The template is compliant with the developments of other technology processes in PIXAPP, therefore making it suitable for assembly and packaging using such state-of-the-art services.
In such a way, the same standard template offers the most efficient use of the available die area and it can be accommodated by all service providers with necessary adaptations with respect to particular technology aspects. This includes the low-entry-cost generic package services with substantial reduction in terms of lead times, reliability and scalability of the incorporated processes (Table 11).

	2018	2020	2022
Platform	InP	InP, TripleX, SOI	InP, TripleX, SOI
Die test service	Semi-automated	Automated, Pilot line	Automated, Test-house
Generic Package	Evaluation Kit	Yes (Cordon, Technobis, LioniX International)	Yes

Table 11 *Roadmap for the JePPIX-PIXAPP standard template for test and packaging.*

2022

The PIXAPP pilot line and its services are expected to be fully operational and accessible to external users supporting volumes up to 1000 units per application annually. The services offered by the pilot line will accommodate small volume demands, which is well suited for MPW run based pilot production. Technologies used in the assembly and packaging pilot line will be standardized but also scalable. The latter will enable package and assembly businesses to take advantage of them and implement them for mid and large volume manufacturing as in the PHIX Photonics assembly line. The scalable processes developed and used in the PIXAPP pilot line will be also implemented by packaging and assembly service providers in the JePPIX consortium (Technobis group, Cordon Electronics, LioniX International).

8.2 Testing

Along with assembly and packaging, PIC testing is another area which forms a significant contribution to the cost of a module and will therefore limit the wide-spread exploitation of PIC technologies. The typical stages in the PIC supply chain are presented in the top row and testing aspects relevant to those stages in the lower row in Figure 16.

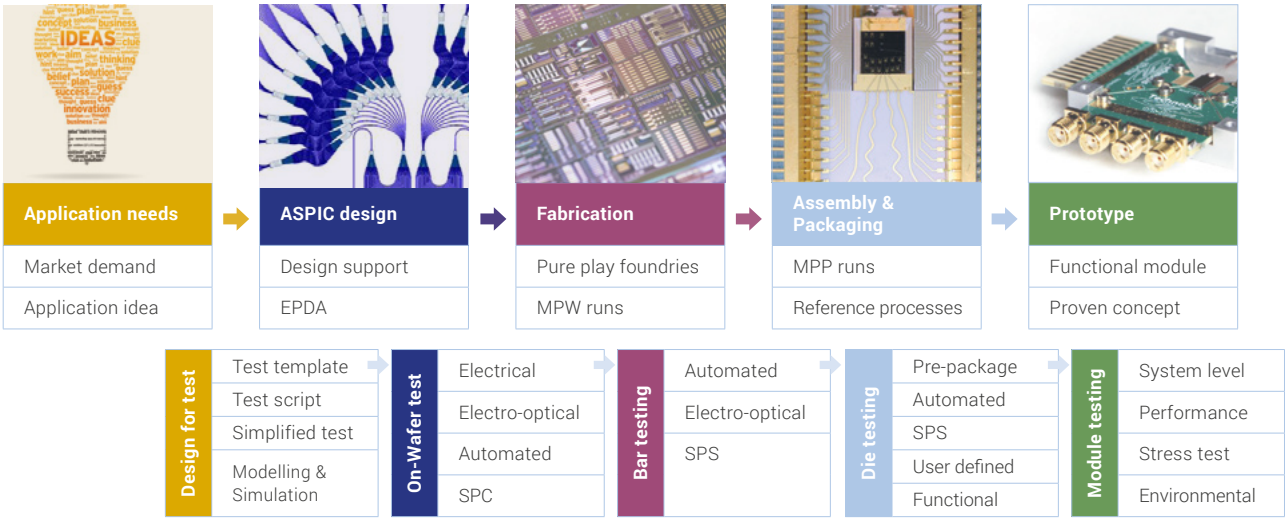

Figure 16 *Testing across value/supply chain of Application Specific Photonic Integrated Circuits.*

Significant R&D effort is required in order to introduce and improve testing at all stages of the PIC supply chain. This will allow manufacturers to optimize and accelerate the whole production process and enable early identification of Known-Good-Dies (KGD). Research and developments towards generic testing of PICs were already undertaken at TU/e in the framework of the PARADIGM project[1]. Wherever possible optical parameters should be measured in an electrical fashion to facilitate fast testing procedures with dedicated test structures relevant to foundry and user sides of test requirements[2], as depicted in Figure 17.

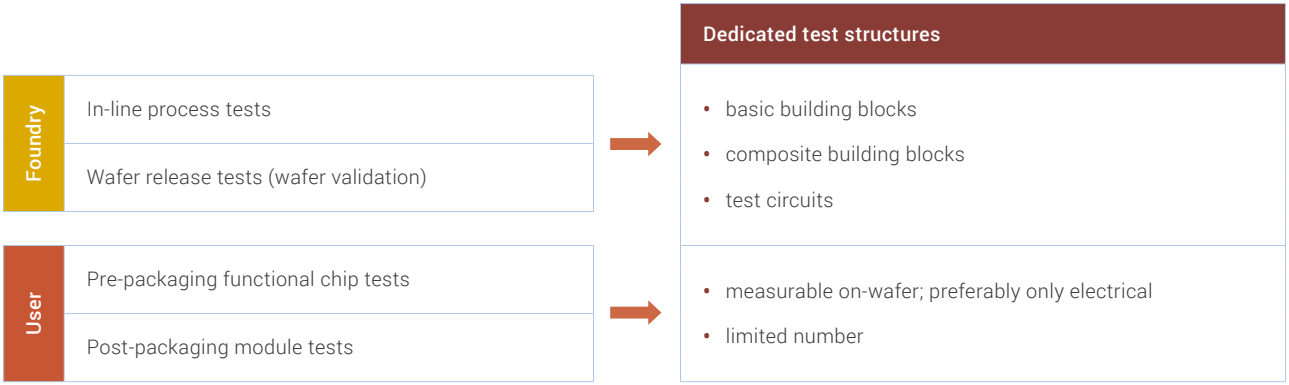

Figure 17 *Dedicated test structures in the context of test demands from foundry and user perspectives.*

Smart testing throughout the production process is required to reduce process spread, center the PIC manufacturing process windows and maximize yield. New inspection methods and analytics are needed to correlate in-line test, off-line product test and product release test in a generic, application independent way. An increased level of automation across the full supply chain will result in a reduction of time required for testing and KDG identification. For wafer verification, on-wafer measurements in both the electrical and the optical domain are desirable to allow for testing at various sites across the wafer prior to cleaving. To this end vertical optical out-coupling structures have to be integrated. Viable options are turning mirrors and grating couplers integrated into appropriate waveguide sections. As of today vertical grating couplers have not been introduced in InP based PICs due to low coupling efficiency; but could still be suitable for testing purposes.

1 E. Bitincka, 'Generic Testing in Photonic ICs,' PhD thesis, TU Eindhoven, 2015

2 N.Grote, 'Workshop on testing of photonic integrated circuits', Pisa 2017

2018

JePPIX Partners have already started work on open access to standardized high-end test facilities for R&D purposes that can also be streamlined to and benefit application-specific processes. In the PIXAPP Pilot line JePPIX is developing state-of-the-art fully automated pre-package die-level test systems and definition and standardization of test protocols according to the timescale presented in Table 12.

	2018	2020	2022
Design for test	Test templates	Supported in design packages User defined test scripts	Automated KGD identification
Wafer level	Electrical Automated	Vertical optical I/O coupling Electro-optical	Self –testing BBs
Bar-level	Basic BBs Manual	Unified processes	Standardized processes
Die-level	Electro-Optical ASPIC-basic (DC) Semi-automated Manual (RF)	Electro-optical ASPIC-functional (DC) Automated DC	Functional Automated (DC,RF) Automated (DC,RF)
Module	Functional	Functional	Functional

Table 12 *Roadmap of open access test at different levels of the ASPIC value chain.*

The Photonic Integration Technology Centre (PITC) at TU/e, in collaboration with industry partners, is developing test methods and automated test solutions across all stages of the PIC value chain. Highly automated testing at wafer-level, bar-level and die-level along with smart testing will enable improvements in statistical process control. Access to a semi-automated test service for MPW-users is expected in 2018. Test houses for photonic integrated circuits will be started; e.g. VLC Photonics starts to offer die- and wafer-level characterization and test services for participants in dedicated and MPW fabrication runs.

2020

A test setup featuring fully automated die handling and fibre alignment sub-systems for performing a number of standard tests on chips fabricated in MPW runs will be offered by the PITC as a part of the PIXAPP pilot line from 2020. The test sequence will be executed according to user predefined test scripts. In the coming years the pilot test facilities will be extended and adopted by industry partners, enabling a path towards testing-as-a-service and support for larger volumes. The increased automation of the processes with implementation of smart testing will have an impact on time required for testing a die allowing for higher throughput.
The expected trend with respect to time needed to test for KGD is presented in Table 13.

	2018	2020	2022
Test time	Hours	Minutes	Seconds

Table 13 *Test time needed for identification of known good die.*

2022

From 2022 the pilot test processes can be replicated and offered by test-houses for lab-less users who wish to assess prototypes before making investments for in-house test equipment. Furthermore, at this point of time those processes are expected to reach an extent of standardization and automation that will substantially foster scalability and volume manufacturing (Table 14). It is expected that from this point on, test methods and equipment at all stages of the PIC value chain starting from design through front-end to back-end will be implemented allowing for implementation of process control modules and manufacturing process optimizations.

	2018	2020	2022
Wafers	Tens	Hundreds	>Thousands
Dies	Hundreds	Thousands	Tens of thousands
Modules	-	Hundreds	Thousands

Table 14 *Annual capacity of test services.*

9. Equipment Roadmap

PIC production is ramping up for high-performance telecommunications links, shipping at levels of hundreds of thousands per month for a number of fabs. Fab capacities handling 3" wafer batches are adequate for such volumes. Discrete devices are produced on 3" and 4" wafers, at volumes of order 10M per month and low complexity PICs comprising lasers and modulators are also ramping up. The current equipment infrastructure is clearly adequate to the cost-performance levels demanded by today's telecom market, but there are increasing concerns that the volumes and costs required by emerging markets, not least data center optics, will put increased pressure on tool performance. Furthermore, the requirement to ramp up faster from first design to production calls for increased tool availability and predictability.

In most cases, InP-fabs can use equipment developed for processing other materials, including silicon. However, it often has special requirements such as the capacity to process 3" or 4" wafers and to handle the less robust InP wafers without damage. It has challenging lithography requirements on line-edge roughness, large depth of focus and extreme critical dimension (CD) control, and the cost of use should match the market size. This requires existing equipment to be adapted to the processing of InP including equipment for wafer handling, epitaxy (layer thickness, composition, defect density), lithography (high resolution), etching (low-damage, accurate depth control, deep etching) and metrology (True 3D and High Aspect Ratio (HAR)).

The III-V group of materials in general and InP in particular is the key material for Photonic Integrated Circuits. This development, today on 3" and 4" wafers is in the ramp-up phase to high volume manufacturing. Larger 6" wafers are commercially available, although with a slightly larger Etch Pit Density, which requires further improvement. In the context of semiconductor manufacturing equipment special attention is required in the following fields:

Front-end-of-line (FEOL) processes:

1. Wafer handling: Due to the fragile nature of InP, fully automated production lines are required. In 2022 we should have completely automated production lines.

2. In-situ measurements are needed to control the layer growth in epitaxy, plasma-enhanced chemical vapour deposition (PECVD) and etch depth control in the etch tools. This should be completed in 2022. In-situ particle detection can be anticipated shortly afterwards.
3. Self-cleaning will be required for epitaxial equipment, and increased reproducibility in terms of layer thickness and composition with control down to +/- 1% in 2022. The introduction of 6" InP wafers for n-type and semi insulating substrates will be considered from 2022 onwards. Demands for epitaxy are given in Table 15[1].

(Epitaxial) growth/layer deposition	[unit]	2022	2025	2030
layer thickness uniformity	%	± 1	± 0.2	± 0.1
layer thickness reproducibility	%	± 1	± 0.2	± 0.1
layer composition uniformity	PL (nm)	± 1 nm	± 0.5	± 0.1
layer composition reproducibility	PL (nm)	± 1 nm	± 0.5	± 0.2
Interface abruptness	nm	1	5/10	3/10
doping concentration uniformity	%	± 10	± 5	± 1
doping concentration reproducibility	%	± 5	± 5	± 1
Other dopant materials	name	C, Be, Mg		
Defect/particle density	cm-2	5	2	1
Wafer diameter	mm	150	150	200

Table 15 *Demands on Epitaxy tool.*

4. Lithography equipment: line-edge roughness, large depth of focus and extreme critical dimension (CD) control will be increasingly important, but there will also be a need to produce circuits with tools developed to match the market size. The demands for the coming period are given in Table 16.

1 Table 15, 16 and 17 have been compiled jointly with the World Roadmap for Integrated Photonics (WRIP).

Stepper/scanner Lithography	[unit]	2022	2025	2030
Overlay accuracy	nm	20	10	5
Resolution	nm	100	50	20
Required Wafer Flatness	µm ttv	0.5	0.2	0.2
CD Loss	nm	10	3	1
CD uniformity	nm	10	3	1
CD reproducibility	nm	10	3	1
Resist thickness	nm	100	100	100
Smallest slot width	nm	100	50	20
Minimum grating pitch	nm	200	180	180

Table 16 *Demands for Optical Lithography.*

5. Etching equipment: depth control and steep side walls, low-damage and deep etching. Overall standardization and optimization of processes is needed. In Table 17 the needs for the etching processes are given.

Dry etching	[unit]	5 years	5-10 years	10-15 years
side wall roughness (rms)	nm	5	2	1
side wall angle accuracy	degree	± 1	± 0.5	± 0.2
etch depth uniformity	%	± 1	± 0.5	± 0.1
etch depth reproducibility	%	± 1	± 0.5	± 0.1
Maximum etch rate	µm/min	5	10	10
CD Loss	nm	10	3	1
CD uniformity	nm	5	3	1
CD reproducibility	nm	10	3	1
Smallest slot width	nm	100	50	20
Smallest line width	nm	100	50	20
Minimum grating pitch	nm	200	180	180

Table 17 *Demands for dry etching tools.*

6. In-line metrology needed in 2020 to measure structures in True 3D and at High Aspect Ratios (True 3D and HARs). It should be possible to measure in-line on-wafer the waveguides, AWG's etc. in real 3D pictures to find failures at an early stage of the processing.

10. Cost Roadmap

For application of photonic ICs in new or improved products the following costs have to be distinguished and will be briefly described below:

- Prototype development costs
- Chip manufacturing costs
- Cost of assembly, packaging and testing

Prototype development cost

For developing a prototype of an Application Specific Photonic IC (ASPIC) the main costs are in the design, the participation in several MPW runs in order to get a prototype fully to specifications, and the characterisation and testing.

The design costs are mainly the salary costs of the designer; they can be significantly reduced by the availability of dedicated Process Design Kits which contain a library with layout and simulation modules for the basic components in the foundry process and software for automatic Design Rule Checking (DRC). Design time is strongly dependent on the complexity of the design and the experience of the designer. Typically it is between a few weeks and several months. While research concepts will yield valuable insights and findings in the first tape-outs, a few fabrication cycles may be required to arrive at a pre-specified performance. In due course the accuracy and the number of the components and sub-circuits supported by the libraries will grow and the design time will reduce accordingly. Eventually first-time-right designs will become feasible for designs that are well within the design rules.

The price for participation in an MPW run is mainly determined by the design area of the chip. The square millimetre cost for an ASPIC design in a TriPleX MPW run is 63 €/mm^2 and for an InP run 240 or 480 €/mm^2 for HHI or SMART Photonics respectively[1]. For this amount the user will receive 2 (HHI), 4 (TriPleX) or 8 (SMART Photonics) copies of his chip. It is interesting to compare these figures with the price of advanced Silicon Photonics platforms which is between €1500/mm^2 and €2000/mm^2 for processes that contain modulators and detectors. InP offers much more functionality (lasers and SOAs included, better modulators) for less than half the price of SiP.

1 Numbers are from 2017.

Platform	Components	MPW run cost			
		Size (mm)	Price (€)	€/mm²	#of chips
HHI Tx 20 Rx 40	DBR and DFB lasers, high speed PDs and PD variants, SOAs, EAMs, current injection PMs, thermo optical PMs, WGs, MMIs, AWGs, Polarization Rotators, SSCs, TBRs, RF pads, ...	4x12	11550	240	2
SMART Tx Rx 10	DBR lasers, SOAs, EAMs, High speed PDs, High speed Mach-Zehnder Modulators, Waveguides, SSCs, MMIs, AWGs, DBR-gratings, RF pads ...	4x4.6	8880	480	8
		2x4.6	4440	480	8
		8x4.6	17760	480	8
TRIPLEX (DS-500-170)*	WGs straight, arcs, tapers, bends, SSCs, Phase Modulators, Y-splitters, Directional Couplers, AWGs, optical beam formers, Mach-Zehnder Interferometers	16x16	16000	63	4
		8x32	16000	63	4
* 50% Academic discount on top of the list price					

Table 18 *Costs of MPW-service for the JePPIX platforms (2018)*

Chip costs in volume production

Scaling laws for InP and TriPleX are similar to other thin film fabrication technologies like CMOS electronics or silicon photonics. Costs are primarily dominated by the amortization costs for the fab, the complexity of the process (number of process steps) and by the loading of the fab. In the case of Silicon Photonics, the reticle costs themselves can be prohibitively expensive for the latest processes, and would need to be shared across a volume of chips, which may explain the relatively high cost of SiP MPWs. Regardless of the technology, increased wafer size and increased throughput of the fab leads to a reduction of the square millimetre price. Figure 19 shows how the square millimetre cost of InP PICs depends on the aggregate annual load of the fab, for different fab scenarios. The load of the fab is expressed in the total number of chips/year for an average chip size of 10 mm^2. For smaller chips the curves will shift to the right, for larger chips to the left.

The first three scenarios are for InP wafer fabs for handling 75, 100 and 150 mm wafers, respectively. The fourth scenario is for a 200 mm fab, which may be a silicon photonics fab offering an advanced process. The fifth scenario is for a small silicon fab carrying a relatively simple process, such as the TriPleX process. The end of the curves indicate the maximum fab capacity.
From the figure we see that for larger fabs the starting costs will be higher, so that higher aggregate volumes will be needed to arrive at low square millimetre costs. The solid lines are indicative for the costs of a 10 mm^2 chip as a function of aggregate chip volumes in a 75, 100, 150 and 200 mm fab.

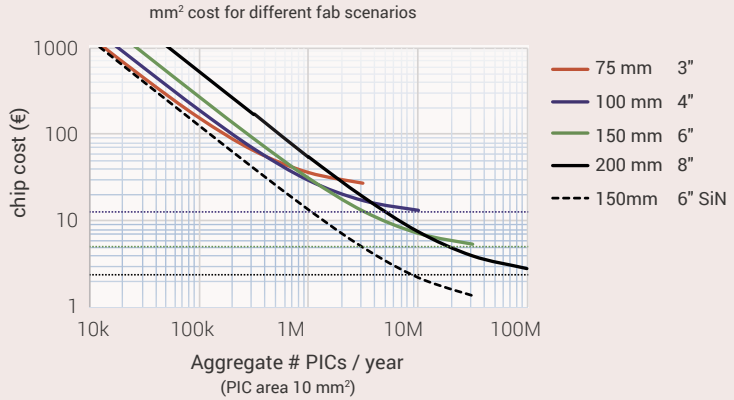

Figure 18 *Chip cost as a function of yearly fab load for different fab scenarios, calibrated for an average chip size of 10 mm^2.*

The graphs are indicative for real chip prices, but they will differ significantly for different implementations of the foundries[1], e.g. whether the fab is highly automated or not. At the high volume end the process costs will be strongly dependent on the complexity of the manufacturing process. Further, yield is an important factor which is strongly dependent on user requirements: if the requirements are well within the building block specifications and the design rules, it will be high. But if they are close to the maximum process performance it can be significantly lower.

Keeping all these reservations in mind we can draw a few conclusions from the graph for InP chips:

- The figure illustrates the advantage of the generic foundry model: because the square millimetre costs are strongly dependent on the total volume, all users of the fab can get their chips at the price corresponding to the aggregate yearly chip volume, while their own chip volume may be much smaller. This will make the costs for small users significantly lower.

1 Details of the model are available from JePPIX.

- For a square millimetre price below 10 €/mm^2, volumes well over 100,000 chips per year are required.
- For a square millimetre price below 1 €/mm^2, volumes well over 1 million chips per year are required.
- The solid graphs apply for both InP and SiP, where SiP uses fabs of 8" and larger. For SiP processes that are largely compatible with CMOS processes, the aggregate volume is for photonic and electronic ICs jointly. If the fab is fully loaded with electronic ICs, SiP can offer low prices already at significantly lower volumes. As most advanced SiP processes differ significantly from standard CMOS real practice will be somewhere in between.
- If the chip volumes are sufficiently high a 10 mm^2 high-performance InP-chip with integrated lasers, SOAs and high-performance modulators, fabricated in a 6" fab[1], will be only a few Euro's more expensive than a Silicon Photonics chip without the lasers and SOAs, while offering significantly more functionality and reduced assembly cost.

Comparison between three major PIC technologies

At present the most important technologies for Photonic ICs are InP-based monolithic integration, silicon photonics (SiP) and silicon-nitride (SiN) technology. InP-based PICs are clearly dominating the PIC market enabling 1.6BE (25%) of the transceiver market today, and expected to account for 3BE (33%) of the market in 2020[2]. Silicon Photonics has a small market share but this is expected to grow, particularly in the datacenter interconnect market sector. Silicon Nitride has a small market but is a promising technology for applications in which low loss is important, for example exploiting microwave photonics, and where visible light is a critical enabler, particularly for bio-sensing. The most important qualities when comparing InP, SiP and SiN are functionality, performance and module cost, they will be discussed below.

Functionality and performance

For passive components SiN has superior performance: losses well below 0.5 dB/cm are available on the MPW platform, with specialised platforms[3] enabling losses below 1 dB/m. SiP and InP have significantly higher losses (1-2 dB/cm). For both SiP and InP losses can be reduced below 1 dB/cm, but not to the level offered by SiN.

1 6" Wafers are presently commercially available and will become a low-cost high-performance solution when the wafer volumes become sufficiently large.

2 Integrated Optical Devices: Is Silicon Photonics a Disruptive Technology? Lightcounting Market Research 2016.

3 J. F. Bauters, et al., "Planar waveguides with less than 0.1 dB/m propagation loss fabricated with wafer bonding" Optics Express 19, 24090 (2011)

For active components InP offers superior performance. It is the only technology that offers the full suite of components including integrated light sources and optical amplifiers. SiP offers good performance for switches and detectors (SiGe), but high-speed modulators suffer from lower electro-optic efficiency and higher optical losses than InP.

Module Cost

For the cost of integrated photonics solutions it is important to distinguish between chip cost and module cost. In many applications, particularly those requiring multiple optical and RF connections, the cost of the chip is only a small part of the total cost of a module, because the assembly and packaging costs are dominant. The technology that can integrate most functionality into a single chip will lead to the largest reduction of the costs of assembly and packaging and the associated loss in performance.

For similar volumes the assembly costs of InP PICs will be lowest. For SiP and SiN PICs the costs of laser(s) and optical amplifier(s) and their assembly with the PIC have to be added to the chip costs. In the example of Figure 18 the dotted horizontal black curve is indicative for chip costs in a fully loaded 8" SiP fab, the blue curve is indicative for the chip cost in a fully loaded 6" InP wafer fab. For the 10 mm^2 chip for which the graph is calibrated, the cost difference is less than 3 €. In order for SiP to be cost-competitive the cost of the laser and the assembly cost must not exceed 3 € and the performance of the module should be comparable. For smaller chips the margin is even smaller.

The cost of hybrid assembly of lasers and optical amplifiers can become low if the volumes becomes very large. However, if the number and the complexity of the lasers that have to be integrated increases, the hybrid solution will become more expensive and will offer less design flexibility and performance (e.g. additional coupling loss) than a monolithic solution. The higher the complexity and performance requirements of the PIC, and in particular the laser source, the larger the advantage of monolithic InP-based integration will be. For highly functional high-performance PICs, e.g. 400 or 1000 Gb/s transceivers using multiple wavelengths, it will be difficult for a hybrid approach to be competitive. Hybrid integration is particularly attractive where a functionality or performance is required that cannot be offered by a single platform, e.g. if active components in combination with very low propagation losses for long delay lines or high-Q filters are required.

11. Public and Private R&D Investment Roadmap

The generic foundry model brings the application of advanced PICs in novel or improved products within reach for many SMEs. The participation fees for MPW runs fit the budget of almost any small sized research project, and in high volumes the chip costs can become very low. An attractive feature of the open-access foundry model is that the chip costs are determined by the aggregate volume of all PIC users. If their aggregate market volume is sufficiently large, they all can benefit from low chip prices, even if their individual market volumes are much smaller.
The generic foundry model thus has a clear societal benefit, especially for smaller companies. In this section we will identify a few priorities for Public-Private funding which will accelerate the development of the eco-system.

The key enabler in the generic foundry model is the generic foundry. For the foundries to become self-sustaining there are two important requirements:

- They should offer access to one or a few platform technologies which support integration of the most important building blocks with a performance which is competitive with application-specific integration technologies.
- The aggregate market volume should be sufficiently large to provide the foundry with an adequate profit margin while at the same time keeping the PIC-costs sufficiently low to be attractive for a large number of applications.

Thanks to a number of large R&D projects (EuroPIC, PARADIGM, MEMPHIS) Europe presently has a unique position with three foundries which organize regular MPW runs in InP and TriPleX technology. These foundries operate at a Technology Readiness Level (TRL) between 4 and 5, which is not sufficient for large scale manufacturing.

Priority 1

As open-access foundries are crucial enablers for the whole PIC ecosystem, moving Europe's unique InP and TriPleX foundries from small-scale TRL 4-5 PIC fabrication to medium and large-scale TRL 7-8

manufacturing should, therefore, be a high priority for both EU public funding and private R&D programs. This will require investments in the order of tens of millions up to a few hundred million Euros over a longer time period. In principle, such investments should best be made at larger PIC manufacturers, which are already capable of handling larger volumes. However, because of the open-access requirement, it will be difficult to involve them because they are usually not willing to provide open access to their processes, so enabling smaller foundries will be a practical choice.

To make the open-access foundries self-sustaining without charging PIC-prices which are prohibitive for broad application, the volume of the PIC market and the number of companies using PICs must be significantly increased. The main barrier here is not the cost of the PIC development, which is in MPW runs affordable to almost every company. Rather the main barrier is a lack of awareness of the potential of PICs for the companies' business, or a lack of knowledge of how to design or test a PIC. So a second priority should be:

Priority 2

A program to reach new PIC users in order to increase both number and volume of PIC-based applications. Without such a program the uptake of the technology may take many years, which is a problem for foundries that have made large upfront investments.

Here projects like ACTPHAST are important, they provide a kind of voucher for having a PIC prototype developed and tested by experts, to companies with a credible business plan. Future initiatives should be focused on methods of reaching a larger number of companies by expanding and intensifying scouting activities, e.g. in support actions like PICs4All, where several Application Specific Centres provide support in different areas of expertise for feasibility of ASPICs. Also the Horizon2020 Pilot Lines offer interesting opportunities for developing novel or improved applications.

The present outreach programs target primarily SMEs and larger companies. It is also important that universities are provided with low-cost access to the technology, in a way as pioneered in the early eighties for microelectronics by the MOSIS project, which is still active today, and has processed more than 50,000 IC-designs since it began. MOSIS gave a huge boost to the development of VLSI design by providing free access to MPW-runs in CMOS processes to PhD students at qualified universities. In Europe Europractice has played a similar role and in Photonics we should establish a similar initiative. A third priority should, therefore, be:

Priority 3

To provide free or low-cost access to MPW-runs to PhD students and other researchers at qualified universities. This may be in exchange for open access library modules of the component or circuit that they have investigated in order to make their know-how available to other researchers and to prevent that everybody has to reinvent the wheel.

This will have a number of impacts. Most of these project will lead to interesting scientific papers, but a number of them will lead to commercial products, and the larger the number of projects is, the larger the number of commercial applications will be. Further it will strongly stimulate the development of a workforce that is capable to design and test PICs. And it may give a large boost to the development of component (IP) libraries which will strongly increase the application potential of the foundry processes by recycling existing knowledge.

Europe has a lead in generic InP-based foundry technology. This is because of strategic investments made by Europe's key players in Photonic Integration through a close cooperation enabled by the JePPIX platform. The US government followed the European Initiative with the AIM Photonics project, a 600 M$ project for developing a US-based photonic foundry capability. Europe has reduced its public funding significantly since the expiration of the PARADIGM project in 2015. Despite of this reduction the foundry infrastructure is being further developed by a mix of private and regional funding. Continuation of smart public-private funding in the coming years is important to reduce the risks in the large investments required for bringing the foundries to a high TRL and strengthening Europe's lead in InP-based foundry technology.

12. Training and Education Roadmap

The rapid growth in the application of PICs across a variety of application areas requires an equally rapid growth of expertise in the field of PIC design, test and measurement.

PIC Design training

A number of universities presently offer PIC design courses. These courses are typically given at a Master degree level. To catch up with the rapid growth of PIC applications it is important that more universities include PIC design for the most important PIC technologies (InP, Silicon Photonics, Silicon nitride and PLC) in the photonics tracks of their Master Programs and that they provide their students with some hands on experience with Photonic Design tools. The EU is planning an ACTPHAST-like project for Researchers, in which academic researchers get low-cost access to advanced Photonic technologies. Such projects will stimulate the growth of the number of researchers with PIC-design experience and will accelerate the introduction of PICs in novel applications.

Co-design of photonic and electronic ICs is becoming increasingly important, not only for high-speed transceivers, but for any high-volume application that requires dedicated control and processing electronics. Without co-design, packaging and testing usually becomes much more expensive, and the performance will be lower.
We consider it of strategic importance that some universities start offering special Master tracks in which students get familiar with the basics of both electronic and photonic IC design.

In addition to the regular curricula, short but intensive design training courses are important for students that want to gain expertise rapidly and for postdocs or senior researchers who want to get skilled in PIC design. JePPIX has been organizing two-weeks photonic IC design training courses at TU Eindhoven each year since 2006. These courses are focused on providing trainee designers with a background in integrated photonics design and technology and practical fab aspects. They include hands-on sessions with various software tools, optical laboratory demonstrations and some basic hands-on experience with processing in the NanoLab@TU/e cleanroom facilities.

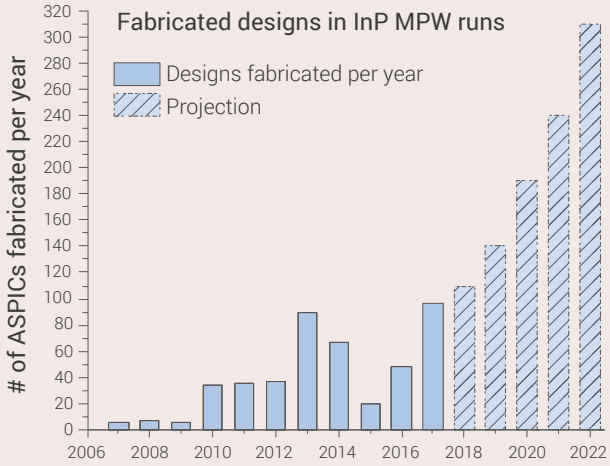

Figure 19 *Overview of ASPICs fabricated per year and projection to 2022.*

This training is focussed on providing the skills for participation in MPW runs. Figure 19 shows the development of participation in MPW runs. It shows a strong dip in 2015 after the transition from free access in the PARADIGM project to commercially priced access. As the commercial fees for InP cells are still very affordable, the interest in InP MPWs is rapidly increasing, up to 60 cells per year in 2017. Considering the rapid increase in application of PICs and the outreach programs that are active to make more researchers and companies aware of the advantages of PICs we expect a steady increase in the coming years, as depicted in the figure.

Starting in 2013 a new type of training has been provided for experienced designers aimed at high level photonic IC design using foundry specific PDKs. These five-day intensive courses have been organized all over the world. Furthermore, JePPIX software partners offer dedicated training sessions to get familiar with the software tools, as well as on-demand practical sessions, and JePPIX is organizing one-day short courses, webinars and workshops in cooperation with design houses as well as 1-3 day customized introductory sessions for specific PIC markets.

Test and measurement is becoming increasingly important now that the complexity of PICs and control electronics is increasing. At present the field is rapidly developing, with emphasis on automated test and measurement, but it is not sufficiently developed yet to justify special educational measures on photonic test and measurement. We expect that in the coming years the demand for test and measurement engineers can be met by providing electronic test and measurement engineers with a basic Photonic Design training, such as the one offered by JePPIX.

Annex 1 | About JePPIX

JePPIX stands for the Joint European Platform for Photonic Integration of Components and Circuits[1]. JePPIX has been extremely successful in bringing the European InP-community together as a coherent force dedicated to building a generic foundry technology infrastructure. Coordination is of key importance for the success of the generic approach since it requires coordination of the work of many independent businesses spread across process development, chip fabrication, packaging, software development, design and training.

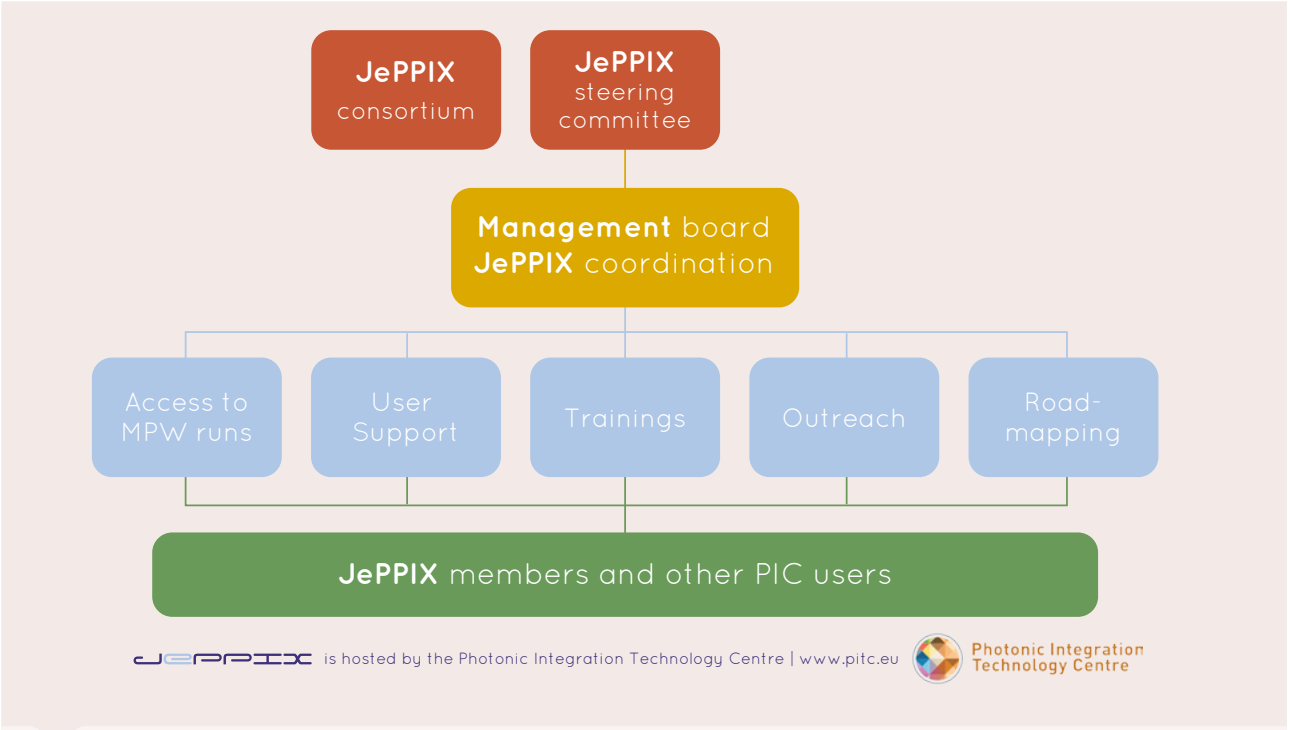

Figure 20 *JePPIX organigram.*

1 JePPIX partners are the PIC foundries Fraunhofer HHI (DE), SMART Photonics (NL) and LioniX-International (NL), PIC-manufacturer Oclaro (now Lumentum, UK), software partners PhoeniX Software (now Synopsys, NL), Photon Design (UK), VPI photonics (DE) and Filarete (IT), design houses VLC Photonics (ES) and Bright Photonics (NL), packaging companies Cordon Electronics (IT), Technobis (NL) and Tyndall (IE), R&D institutes III-V Lab (FR), Politecnico di Milano (IT), TU Berlin (DE), and the Photonic Integration Technology Centre (PITC, NL). The PITC is hosting JePPIX.

The JePPIX platform is presently recognized as the coordinating body by all the key players in the InP-based foundry approach and it is, therefore, the instrument par excellence for coordinating future development. Because of the high degree of complementarity between InP technology and low-loss dielectric waveguide technology for a range of applications, and the organizational similarity in handling MPW runs, JePPIX is supporting both InP and TriPleX technology.

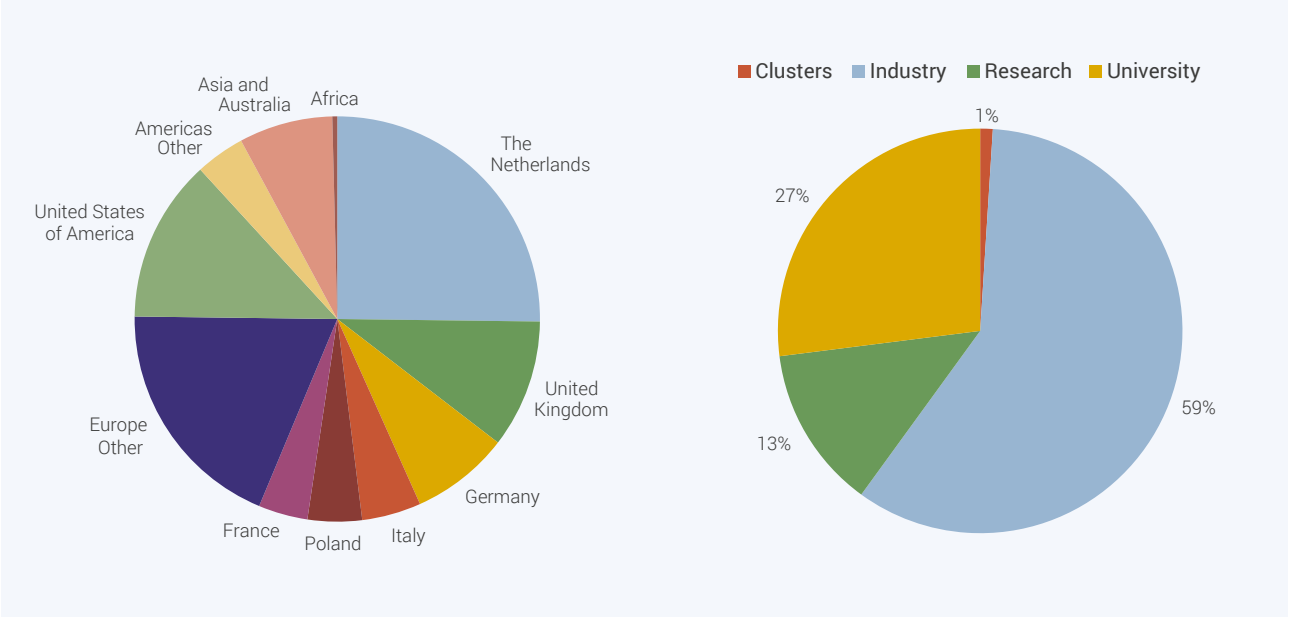

Figure 21 *JePPIX members and their country of origin. Currently the JePPIX membership list counts more than 300 members.*

The structure of JePPIX is represented in Figure 20, JePPIX is managed by a management board, which includes a full-time coordinator. The management board together with the JePPIX Steering Committee take the decisions concerning the main activities happening within the ecosystem, the SC provides for broad representation of the partners that contribute to the technological infrastructure, including representatives of the user and the designer communities.

JePPIX is hosted by the Photonic Integration Technology Centre and runs the following activities:

- **Organization of MPW runs** on the three generic foundry processes that are presently available in the platforms. It includes supplying the design kits and other design information and handling legal aspects (NDAs and licenses).

- **Education and training.** JePPIX organizes international and in-house yearly training courses in photonic IC design and technology and it is presently expanding its training offer in cooperation with its software partners to offer webinars and workshops.

- **Roadmap.** JePPIX publishes a roadmap for technology development, applications development, cost and market development, education and training, and R&D investments. The roadmap is updated every two or three years.

- **User and member platform.** JePPIX is building a member group of companies, universities and research organisations to create the technology eco-system and the value chain to reduce entry barriers to ASPIC development. JePPIX provides members with information and support for participation in foundry runs and information on applications for ASPICs. At present JePPIX has more than 300 members: companies, universities and other organisations. Figure 21 shows where they come from. A significant proportion of JePPIX members is formed by industry, both SMEs and large companies.

- **Outreach activities.** JePPIX is actively extending its outreach to SMEs and large companies throughout Europe. This activity includes the JePPIX mentoring program as well as scouting promotions and active participation in international conferences and exhibitions.

- **Regional support centres.** JePPIX stimulates the creation and operation of regional support centres worldwide for reaching out to potential users and helping them to find their way on the path to application of ASPICs. The support covers design, manufacturing and testing of photonic ICs.

JePPIX membership is free. For more information about JePPIX or for becoming a member see **www.jeppix.eu**.

Annex 2 | Survey 2017

This report summarizes the results of the JePPIX Survey on Generic Photonic Integration Platforms based on InP, which was conducted throughout 2017. The survey consists of a set of questions prepared through a web-based tool and has been filled by participants having extensive technical knowledge on (part of) the subject matter. For some detailed questions the number of respondents was too low to draw conclusions and the outcomes should be considered as indicative only.

Objectives

The objective of the survey was to gather input from participants about the requirements they have on photonic integrated circuit (PIC) technology, and to use the information for the present JePPIX Roadmap and technology development choices. JePPIX uses the survey to assess the technical requirements of PIC users on the generic platform technology. Specifically, it is of interest which components are most required by users and what specifications are desired for them. The results have enabled JePPIX to better focus its technology development towards user needs and increase the impact of generic InP PIC platforms. In addition, the survey gives information on emerging application areas and provides indications for pricing and volume demands.

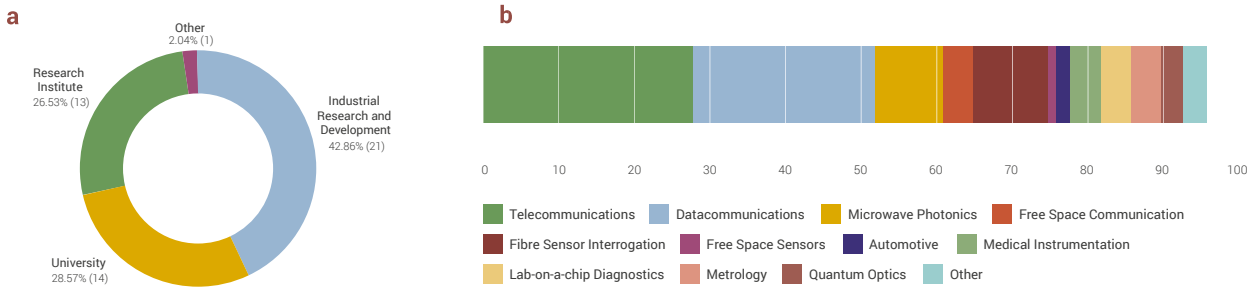

Figure 22 ***a*** *Distribution of survey respondents (49 replies).*
b *Application areas (represented by percentage of 36 total replies) that are of interest for survey respondents.*

General Results

The respondents that took part in the survey came both from academia and industry. Figure 22a shows the distribution, indicating that 21 of the 50 participants represent companies that are involved in industrial research and development whereas the rest are employed in research institutes or in universities. This ensures a balanced representation of both industry and academia in the results of the survey. PIC technology has been mainly used in telecom and datacom applications so far and this is also evident here when respondents were asked for their application field of interest. The results shown in Figure 22b indicate that more than 50% of the respondents are interested in telecom and datacom applications. From the list of potential new applications that can benefit from PIC technology Microwave Photonics and Fibre Sensing are mentioned most frequently.

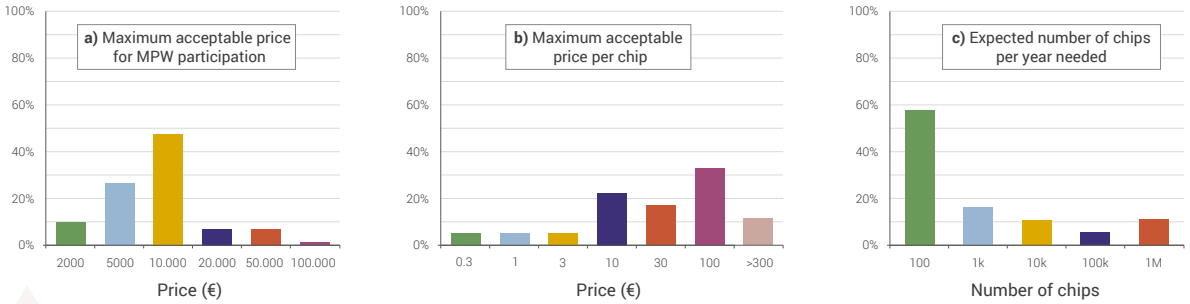

Figure 23 *Indications on acceptable price per MPW and per chip and expected chip volumes of respondents. Total number of replies for (a), (b) and (c) are 30, 18 and 19.*

Figure 23a and Figure 23b show the results for the cost of participation in a multi-project wafer run and the cost per chip in volume manufacturing that the respondents considered acceptable. Figure 23c indicates the estimated number of chips for the applications targeted by the respondents. It is evident that most respondents accept a MPW participation price of up to 10,000 €. The majority of respondents only need 100 chips per year and only two of the respondents (10%) expect to need millions of chips per year.

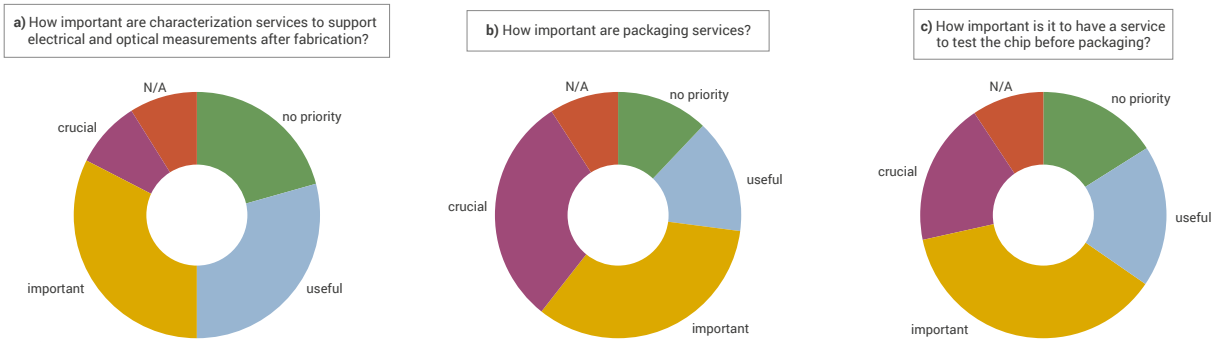

Figure 24 *Indication of importance of characterization and testing services. Total number of replies for (a), (b) and (c) are 34, 33 and 32.*

The photonic chip is only one part of the user's end product and needs to be properly tested and put in a product assembly or package after it comes out of the fab. The respondents were asked about their need for testing and packaging services and the results are shown in Figure 24. About 40% find a characterization service after fabrication crucial or important. More than half find it crucial or important to have packaging services for the chips. Also more than half find it crucial or important to have a test service before packaging.

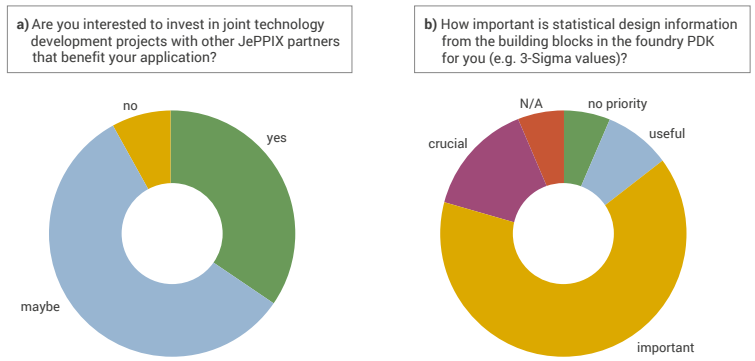

Figure 25 ***a*** *Interest in joint technology development and* ***b*** *in statistical data for offered building blocks.*

The generic PIC platforms offer standardized technologies and building blocks that can fit many applications. However, for some application fields technology enhancements or extensions will be needed to add capabilities or improve performance over existing technology. Respondents were asked if they are interested in investing in joint technology development with JePPIX partners to tackle that and the results are shown in Figure 25a. More than half indicate that they are potentially

interested. To get to a good circuit design, a rich and accurate process design kit (PDK) is required. When asked how important statistical design information within the PDK is, more than 75% of the respondents say it is crucial or important.

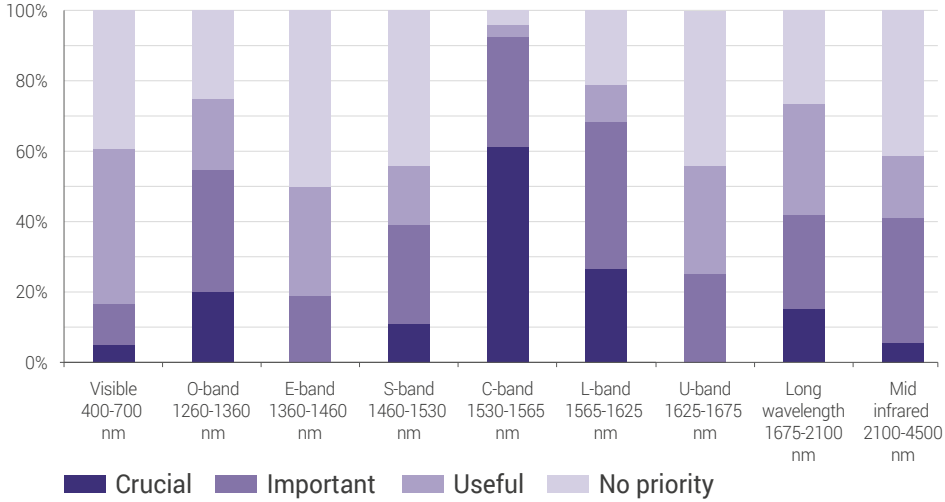

Figure 26 *Indicated importance of different wavelength bands for respondents (28 answers).*

The JePPIX InP foundry platforms focus on C-band applications. Respondents indicate that this is indeed the most relevant wavelength range as shown in Figure 26. Second in importance is the L-band from 1565-1625 nm. There is also interest in the O-band and long wavelength and mid infrared wavelength ranges.

As the PIC platforms offer a variety of basic building blocks, proper prioritization and focus on developing the most important ones from the user's perspective is important. We asked the respondents to indicate if they would like to answer in-depth questions for each building block. The results are shown in Figure 27a. They indicate the preference for a certain building block. Passive components are the main interest of the respondents. This is not surprising as it is a collection of various building blocks, shown in Figure 27b. Within passive components, the main interest of the respondents is in waveguides, AWGs, MMIs and polarization handling devices.

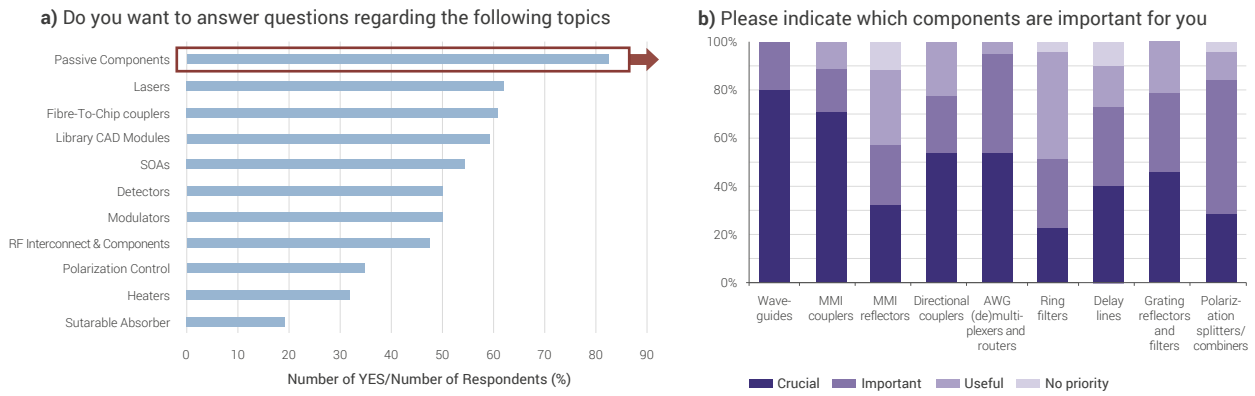

Figure 27 ***a*** *Preference to answer questions regarding a certain building block.*
b *Importance of several passive components. Total number of answers in (a) are between 21 and 29 and in (b) are 19.*

Next to passive components, also lasers, fibre-to-chip couplers, library CAD modules, SOAs, Modulators and detectors are important for more than half of the respondents. Library CAD modules should contain the layout information together with supporting measurement and simulation data and compact models for a given building block, encapsulated within the PDK and accessible through design software. We asked furthermore which components should be represented in such library CAD modules and the results are shown in Figure 28. For almost all components more than half of the respondents find it crucial or important to have library CAD modules. In particular, for phase-modulators, MMIs, AWGs, Bragg reflectors, mode field adaptors and tunable lasers, more than 90% find it crucial or important to be able to access library CAD modules.

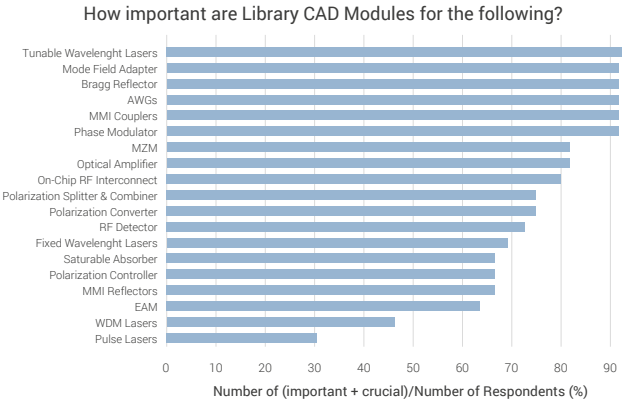

Figure 28 *Indication of importance of library CAD modules. Number of people finding it important or crucial.*

In the following, results on more specific questions related to different building blocks are presented.

Passive Components

More than half of the respondents indicate 0.5 to 1 dB/cm as acceptable passive losses for waveguides. For MMI-couplers more than 75% of the respondents indicate 0.2 or 0.5 dB as acceptable insertion loss value and 0.1 dB as imbalance value. Spurious reflection values up to -30 dB are regarded as acceptable by more than 90%. Only about 30% requires a variable splitting ratio for the couplers. For AWGs, 20% need 40 or more channels whereas the rest is satisfied with 4 channels or more. More than half of the respondents is satisfied with 50 GHz minimum channel spacing and 2 dB as insertion loss. Adjacent channel crosstalk should be below -25 dB say more than 60% of the respondents.

Lasers

50% of the respondents indicate that 3 to 10 mW is their minimum required output power. 43% need 10 nm and 36% need 40 nm tuning range. The remaining respondents would like to have 100 nm tuning range. 83% are satisfied if the tuning speed is between 10 and 100 ns. More than half of the respondents need laser linewidths lower or equal to 300 kHz and more than 60% wishes maximum operating temperatures above 70 degree Celsius.

Mode-Field Adapter

About 70% of the respondents desires a 10 µm large mode field diameter. About half of the respondents accept 1 dB as insertion loss and 0.2 dB as polarization dependent loss. Only 40% find it crucial or important to have normal direction out-couplers. 70% indicate that 250 µm is the preferred pitch.

SOAs

More than half of the respondents indicate that 20 dB is the desired amplification of SOAs with 100 cm^{-1} modal gain. About one in three respondents require 10 mW of 3dB-saturation output power and about three in four want maximum operation temperatures of 70 degree Celsius or above.

Detectors

50% of the respondents require 50 GHz small signal modulation bandwidth for detectors and about 45% need balanced detectors. More than 75% accepts 10 to 50 nA of dark current and 60% require 0.9 A/W responsivity. 70% want to have 10 mW or more of maximum input power.

Modulators

About 70% of the respondents need more than 25 GBd of modulation speed and about 50% want 35 to 65 GHz of modulation bandwidth. More than 60% accept insertion loss of 2 dB or more and 50% want 15 dB or more static extinction ratio. 70% can tolerate 2V or less of drive voltage and more than 80% can tolerate a footprint of up to 1 mm in length. Two in three respondents indicates that chirp should be kept at 1 GHz or below. Mach-Zehnder type modulators are preferred over other types.

RF Interconnects and Components

More than half of the respondents need interconnect bandwidth to be 50 GHz or above. About three in four require only a length of 1 mm or less to be bridged by RF interconnects. 50% find integrated 50 Ohm terminations to be crucial or important.

Polarization Control Elements

Acceptable insertion loss is 0.5 dB say two out of three respondents. More than half of the respondents find integrated polarization splitters or combiners important or crucial and 40% need 30 dB polarization selectivity.

Conclusions

The results of the JePPIX Survey 2017 have given us valuable information on the requirements for PIC platforms both from industry and academia. The main application areas are in the telecom and datacom field with fibre sensing and microwave photonics gaining weight. Pricing of 10 K€ for MPW participation seems acceptable and chip prices can be up to 100 Euro per chip for a number of applications in which PICs offer a high added value.

This conclusion applies mainly to users that do not require high volumes yet. Packaging, and test before packaging services are crucial and so is statistical building block information in PDKs. The respondents gave important indications on where to focus future component and technology development and also presented us with required specification values for each building block. Although the number of respondents does not allow us to draw firm conclusion for all the questions, their replies indicate important trends and opinions which have helped to shape the 2018 roadmap. It is our prime aim to continue and update this survey in future to better steer and improve the offer of JePPIX.

Annex 3 | List of Abbreviations

ACTPHAST	EU project for supporting photonic innovation
ALD	Atomic Layer Deposition
ASPIC	Application Specific Photonic IC
AWG	Arrayed Waveguide Grating
BBB	Basic Building Block
BEOL	Back End of Line
CAD	Computer Aided Design
CAGR	Compound Annual Growth Rate
CBB	Composite Building Block
CD	Critical Dimension
CMOS	Complementary Metal Oxide Semiconductor
DBR	Distributed Bragg Reflector
DC	Direct Current
DFB	Distributed Feedback
DRC	Design Rule Checking
DUV	Deep Ultra Violet (193 nm)
DWDM	Dense Wavelength Division Multiplexing
EAM	Electro-Absorption Modulator
EOPM	Electro-Optic Phase Modulator
EPDA	Electronic Photonic Design Automation
EPIXnet	FP6 Network of Excellence
Europractice	EU-based microelectronics MPW brokering organisation
FBG	Fibre Bragg Grating
FDM	Frequency Division Multiplexing
FEOL	Front End of Line
FhG	Fraunhofer Gesellschaft
GDSII	Mask Layout standard
HAR	High Aspect Ratio
HHI	Heinrich Hertz Institute
IPI	Institute for Photonic Integration (TU Eindhoven)
IC	Integrated Circuit
InP	Indium Phosphide

IoT	Internet of Things
KGD	Known-Good-Die
LIDAR	Light Detection And Ranging (Optical Radar)
MMI	Multi-Mode Interference
MOSIS	US-based microelectronics MPW brokering organisation
MPW	Multi Project Wafer
MZ	Mach Zehnder
OCT	Optical Coherent Tomography
PDK	Process Design Kit
PD	Photo Diode
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PIC	Photonic Integrated Circuit
PIN	P-type / Intrinsic / n-type junction
PITC	Photonic Integration Technology Centre
PIXAPP	EU Packaging Pilot Line (run by Tyndall Institute)
PLC	Planar Lightwave Circuits
PM	Phase Modulator
PZT	Lead Zirconate Titanate (piezo-electric ceramic material)
Rf	Radio Frequency
RoF	Radio over Fibre
Rx	Receiver
SDL	Schematic Driven Layout
SiGe	Silicon Germanium
SiN	Silicon Nitride
SiO_2	Silicon dioxide, silica
SiP	Silicon Photonics
SME	Small or Medium Enterprise
SOA	Semiconductor Optical Amplifier
SPC	Statistical Process Control
SSC	Spot-Size Converter
SSMF	Standard Single Mode Fibre
TriPleX	Brand name for SiN waveguide fabrication process
TRL	Technology Readiness Level
Tx	Transmitter
UPH	Units per hour
WDM	Wavelength Division Multiplexing
WG	Waveguide

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Photograph Cover: Panoramic view of a processed InP multi-project wafer. Image by F. Lemaitre
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