Heat sinking of highly integrated photonic and electronic circuits

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Dense integration of photonic and electronic circuits poses high requirements on thermal management. In this paper, we present analysis of temperature distributions in PICs in InP membranes on top of a BiCMOS chip, which contains hot spots in both the photonic and the electronic layer (lasers, optical amplifiers, driver electronics) and show that with proper design of surrounding structures both layers can be sufficiently cooled.

Introduction

Currently, photonic integrated circuits (PICs) are electrically connected using wire bonds. However, these wires are expensive to place in large numbers and physically large compared to the chips they connect, limiting design freedom in chips as well as the potential information capacity of these designs [1]. Wafer scale integration of photonics and electronics is a cost effective solution to the increasing demand for high speed optical communication by enabling the creation of high-density, high performance electro-optical modules. This is achieved in a new concept, called photronics, where we bond a thin InP membrane containing a complete PIC on a BiCMOS chip using an adhesive polymer and electronically connect the two layers with wafer-scale processing [2], as shown in fig. 1. This novel integration scheme allows for very short, high bandwidth interconnections, and a greater freedom in the placement of interconnections.

One major challenge for this integration scheme is the simultaneous cooling of both layers. It is especially important that the photonic layer is cooled to and stabilized at a temperature that allows stable operation of lasers and other photonic components. Furthermore, the underlying electronics should not be affected by the hot spots in the photonic InP layer. In this paper we will investigate the thermal properties of an integrated transmitter chip with an electronic driver section in the BiCMOS and a laser in the InP PIC.

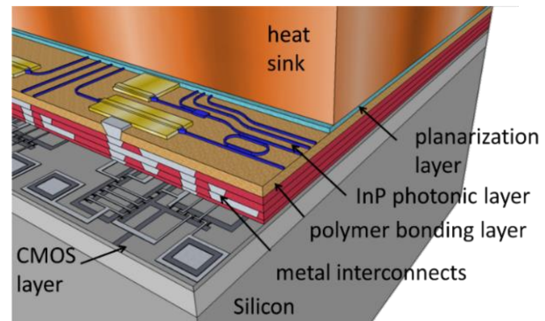

Fig. 1. Artist impression of complete photronics chip, combining both a BiCMOS

Goal

Hot-spots can be identified at the surface of both the BiCMOS and InP chips. In these region, upon device operation, the temperature increases substantially with respect to the surroundings. The goal of our study is to determine how the local temperature increase in the hot-spots affects the electro-optic operations of the photronic assembly. Further, we study the effect of heat spreading structures. The overall structure and design of the chip and these additional structures is shown in fig. 2 and 3 and further explained in the next section.

The maximum temperature at which a BiCMOS chip can still operate without loss of function is typically 150°C, so the BiCMOS chip should remain below that temperature. The maximum temperature at which a lasers and optical amplifiers can be operated are dependent on the specific

application. Typically phosphorous-based lasers can be operated at junction temperatures up to 70-80 ºC, and Al-based lasers at temperatures up to 90-110 ºC, although performance will be reduced compared to room temperature operation [3]. So, for our simulation we will aim to bring the junction temperature below 110ºC, although lower temperatures are greatly preferred.

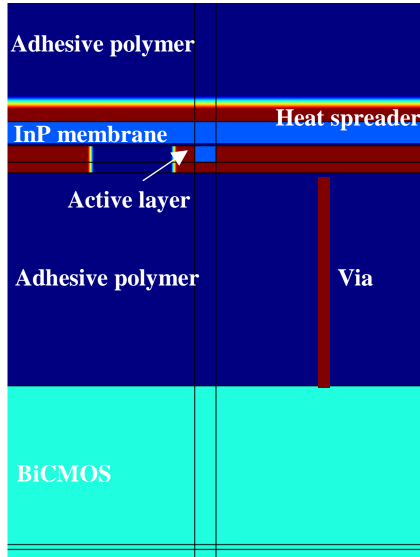

Fig. 2. Cross section of photronics chip showing both the top of the BiCMOS layer and the InP PIC.

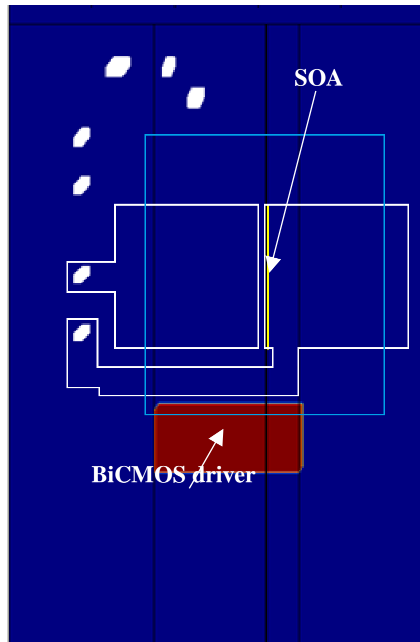

Fig. 3. Top view of thermal simulation showing both heat sources, the metal between the InP and the BiCMOS in white and the heat spreader in light blue.

Simulation set up

To simulate the thermal behavior of a photronic chip it is important to include all relevant boundary conditions and the full 3D behavior of the chip. Therefore we created a 3D finite elements method simulation where the chip is sandwiched between several thermal interface materials with a passive heatsink on both the top and the bottom of the chip. This double-sided heatsink approach was chosen to minimize the thermal crosstalk.

In fig. 2 we see the cross section of the photronics chip. The bottom of the figure shows the top layers of the BiCMOS chip, where the thin layer near the bottom is the active layer of the chip with the heat generating transistors with the metal layers on top. The InP layer shows the InP membrane over the entire width of the chip with the active layer and the p-InP extruding downwards. The red layer connected to the p-InP is the p-contact with next to it the n-contact. The red layer on top shows the location of a potential heat spreader that might be added to distribute the heat of the laser over a larger area.

The top view of the simulation is shown in fig. 3, including the power sources on both the BiCMOS and the InP and the patterns of the metal near the InP. The red rectangle depicts the location of the heat source on the BiCMOS, dissipating 380 mW of heat. The yellow line shows the location of the laser, which dissipates 290 mW. The white shapes indicate the metal between the InP and the BiCMOS, where the solid white circles are vias connecting the two. The light blue rectangles is the heat spreader on top of the InP. Toward the top of the chip there is a passive section without heat sources or metal layers (not shown). This adds additional area to connect to the heat sink.

There are a number of design parameters we can vary to improve the thermal behavior of the chip. In this paper we will investigate the effect of the thickness of the InP membrane on the temperature inside the laser cavity, with or without a 2 μm thick gold heat spreader. We also will investigate changes to the thickness of the heat spreader for a number of different materials. Optimizations on the size of different metal pads are still ongoing, and the largest feasible sizes are used in this paper.

Results

To investigate feasible configurations we first simulated the effect of the varying design parameters on the temperature inside the laser cavity, given that the ambient temperature is 25°C. As seen in fig. 4a, it is not practical to create this chip without a back side heat spreader. A 2 µm thick gold heat spreader is sufficient to lower the temperature to a level that would be acceptable for an Al-based laser, although lower temperatures would improve the performance of such a laser.

Fig. 4b shows the effect of increasing the thickness of the heat spreader from 2 µm to the full thickness of the top adhesive polymer layer, 20 µm, for a number of materials. For example, 0.35 W/m K is the thermal conductivity of the polymer, 10 W/m K is that of a thermal paste, 68 W/m K, 150 W/m K, and 320 W/m K are the thermal conductivities of InP, Si and gold respectively. We can see that a 4 µm thick gold heat spreader would reduce the temperature to a safe level for Al-based lasers and that a heat spreader of 10 µm thick gold or 20 µm thick Si is needed to use a phosphorous-based laser. We expect that we can achieve a result similar to 4 µm thick gold using 2 µm of gold and 18 µm of thermal paste.

A further exploration of the thermal behavior of the chip with a 2 µm thick gold heat spreader is presented in fig. 5, where we can see the effect of both heat sources on their own layer (fig 5 b and c) and the cross talk to the other layer (fig 5 a and d). Here we see that BiCMOS is well below the maximum allowable temperature with only limited cross-talk from the laser source. We also note that temperature of the InP membrane is mainly determined by the heat dissipated by the laser.

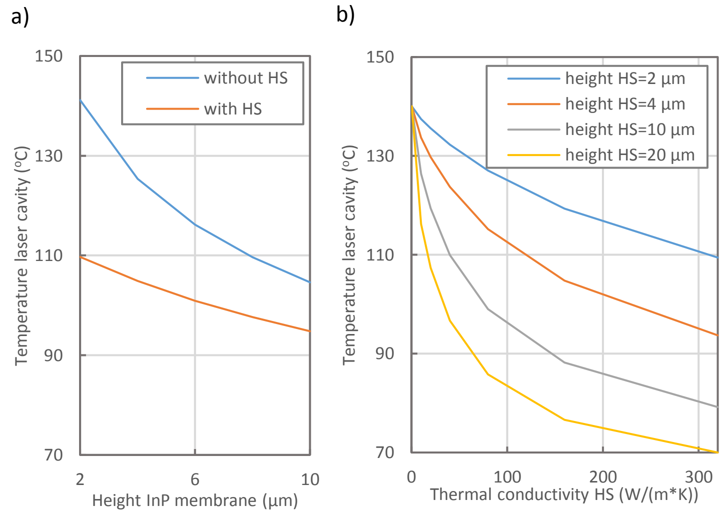

Fig. 4. a) Shows the impact of spreading the heat using the thickness of the InP membrane or a thin gold heat spreader on the temperature of the laser. b) Shows to impact of different materials and thicknesses of the heat spreader.

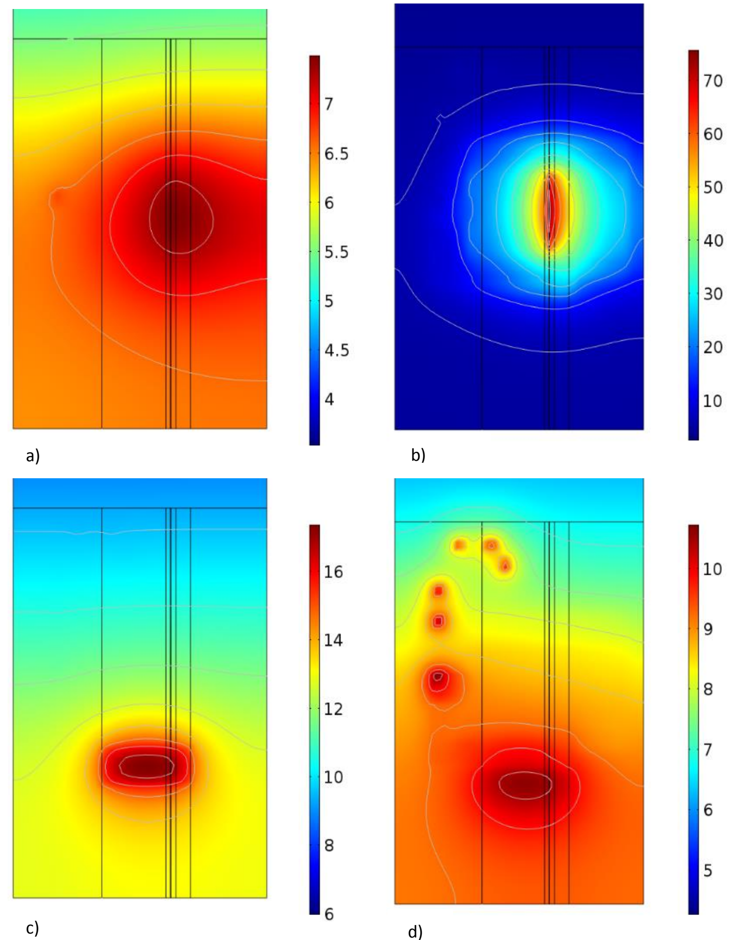

Fig. 5. Temperature increase (K) of a) the B iCMOS due to the laser, b) the InP due to the laser, c) the BiCMOS due to the driver, d) the InP due to the driver.

Discussion and conclusion

For a proper discussion of the results it is important to briefly discuss the impact of these changes on the fabrication process. Changing the thickness of the InP membrane means that a thicker InP layer needs to be grown, resulting in more defects in the material. This means that it is greatly preferred to keep the InP membrane as thin as possible. Our results show that it is possible to use the 2 µm thick InP membrane.

Some form of heat spreader is necessary for a working laser. The 2 µm thick gold heat spreader can be added in the same step as the vias after the bonding process, which means adding such a heat spreader is not a problem from a process stand point. However, increasing the thickness of the heat spreader will require additional production steps. One concern about adding the heat spreader is that it will introduce additional stresses in the InP membrane, which might lead to defects.

To conclude, we simulated the thermal behavior of a novel photonic-electronic integration scheme, where we adhesively bond a thin InP membrane containing a complete PIC on a BiCMOS chip and electronically connect the two layers with wafer-scale processing. In this simulation analysis we found that we are able to sufficiently cool the BiCMOS without taking additional measure to cool the chip. The cooling of the laser is more complicated, since the heat generated by the laser cannot spread through the thin InP membrane or the surrounding polymer. This can be solved by using very large metal contacts and adding a gold heat spreader on top of the InP membrane of at least 2 µm thick. Further cooling can be achieved by increasing the thickness of the heat spreader to 4 µm or by replacing the polymer above the laser with thermal paste.

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References

[1] S. Kanazawa et al., "400-Gb/s operation of flip-chip Interconnection EADFB laser array module", *Proc. Opt. Fiber Commun. Conf.*, 2015.

[2] European commission, http://cordis. europa.eu/project/rcn/199492_en.html

[3] M. Silver et al., "Wide Temperature (-20ºC -95ºC) Operation of an Uncooled 2.5-Gb/s 1300-nm DFB laser", *IEEE Photon. Technol. Lett,* vol. 14, no. 16, June 2002