

Photonic Electronic Integration at Wafer Scale

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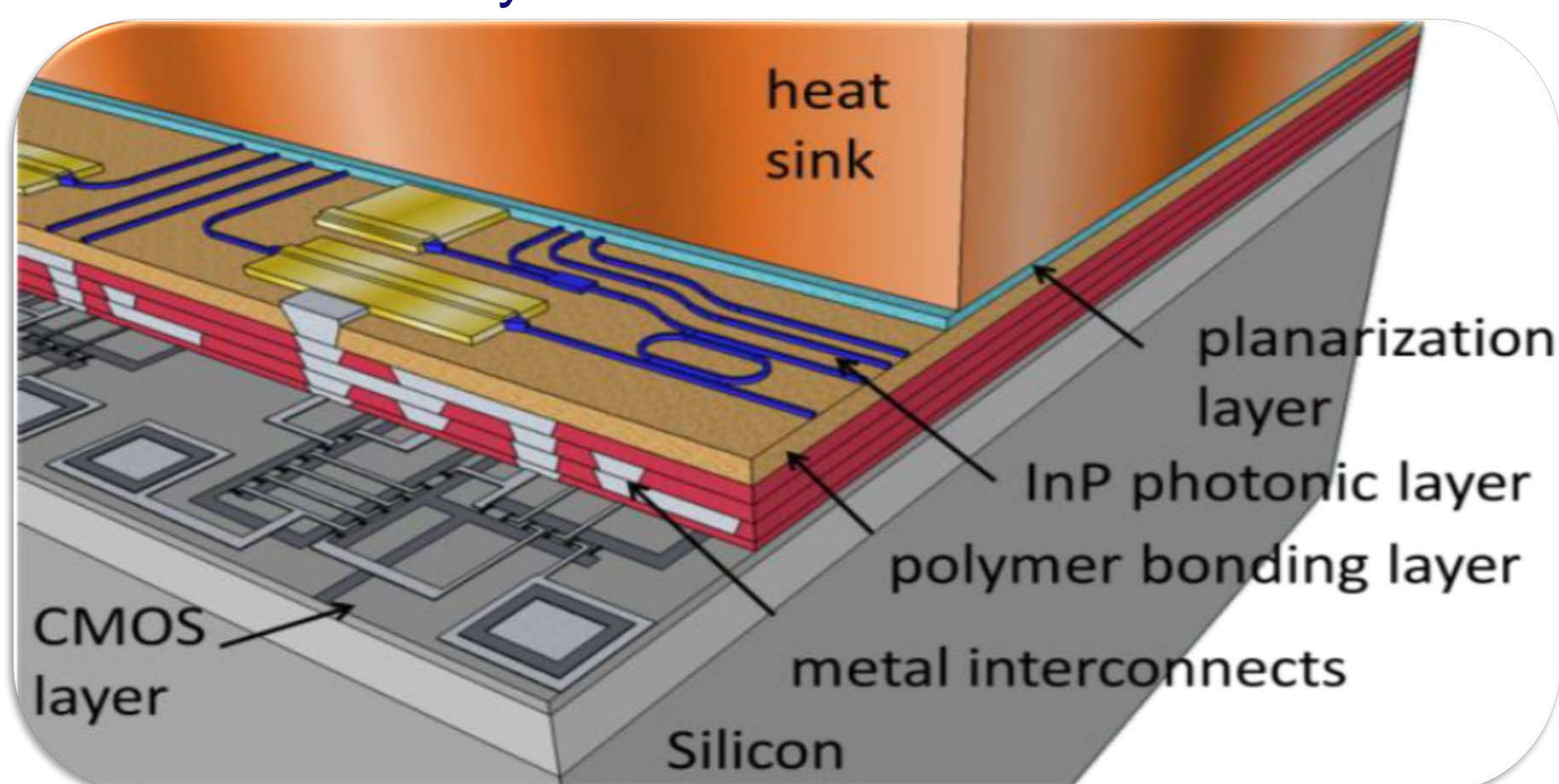
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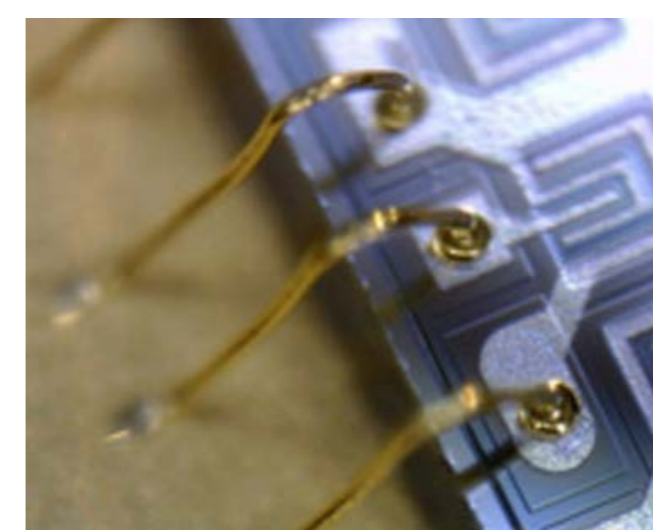


Introduction

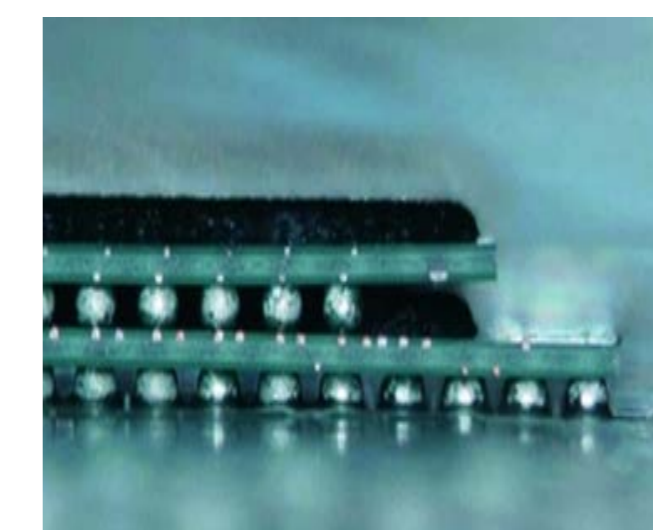
Single-chip photonic-electronic integrated circuits will outperform discrete electronic-optical systems in terms of physical size, ease of assembly and bandwidth density.



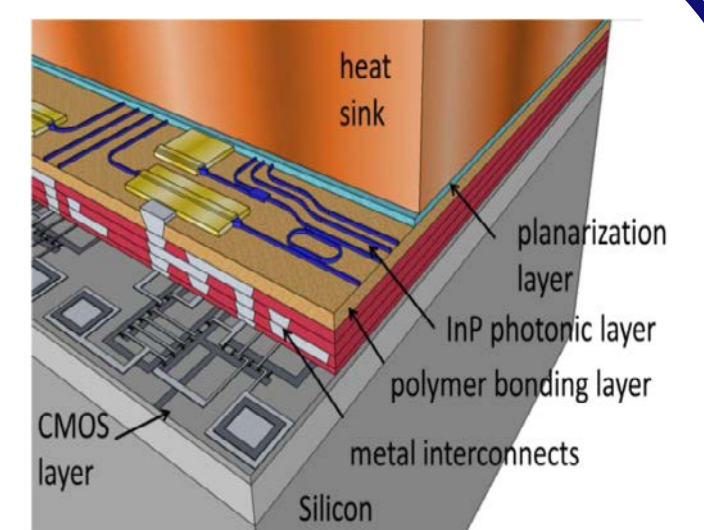
Technology Comparison



Wire bonding



Flip-chip



Wafer-scale Fabrication

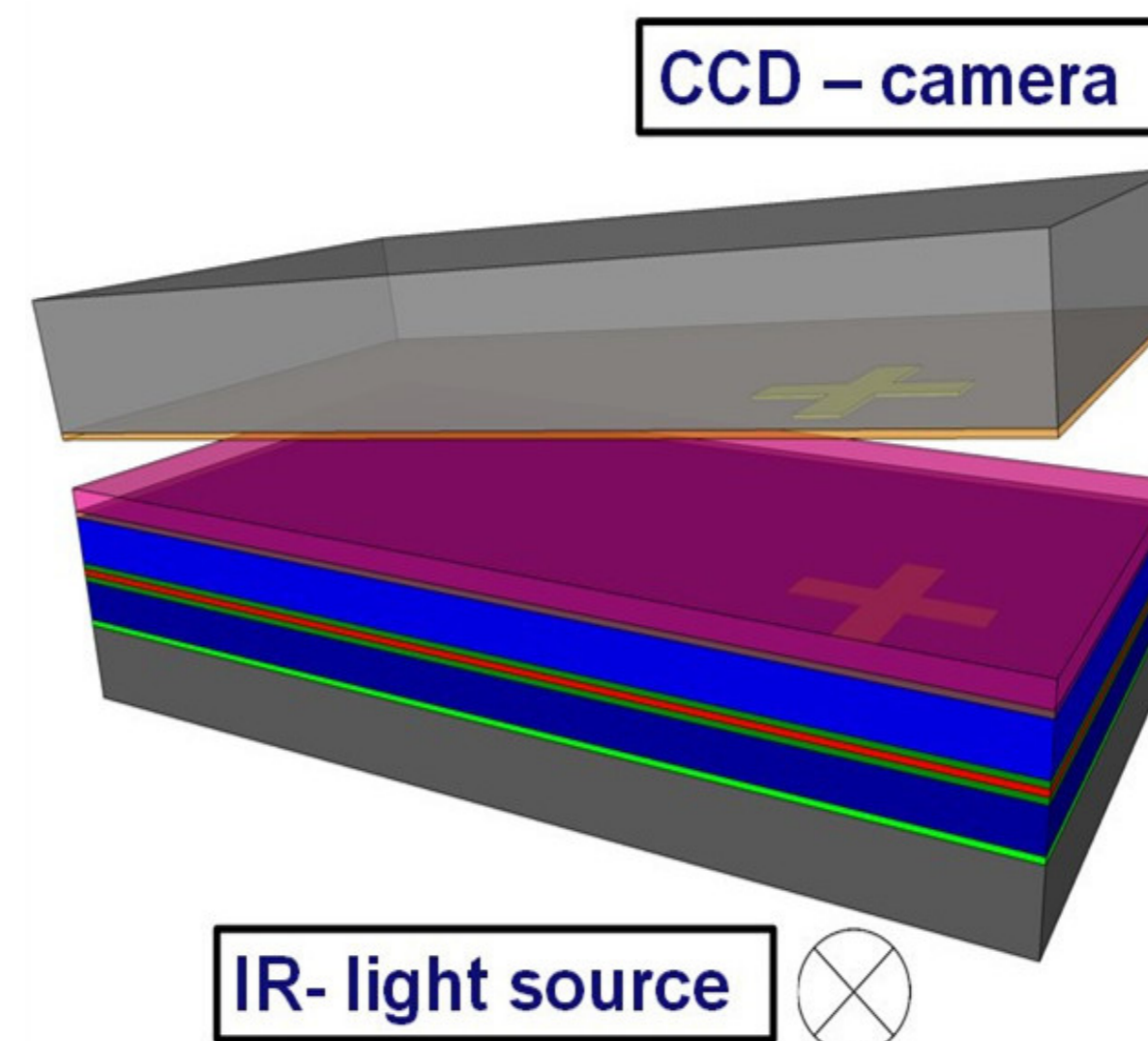
Advantages of wafer-scale fabrication:

- ✓ New design freedom in optical waveguide design
- ✓ Using mature InP technology without interfering with the processing of the BiCMOS chip
- ✓ Short interconnections: suitable for very high speed operation at low energy consumption
- ✓ New design freedom in electronics and photonics co-design

Technical Flow Process

- Step 1**
 - Produce BiCMOS wafer
 - Produce InP photonic wafer
- Step 2**
 - Align BiCMOS wafer and InP wafer
 - Bond two wafers by polymer
- Step 3**
 - Remove the photonic substrate
 - Process optical I/O on the Photonic layer
- Step 4**
 - Perform interconnect metallization between the photonic layer and BiCMOS metal layer
 - Create electronics I/O through the photonic layer

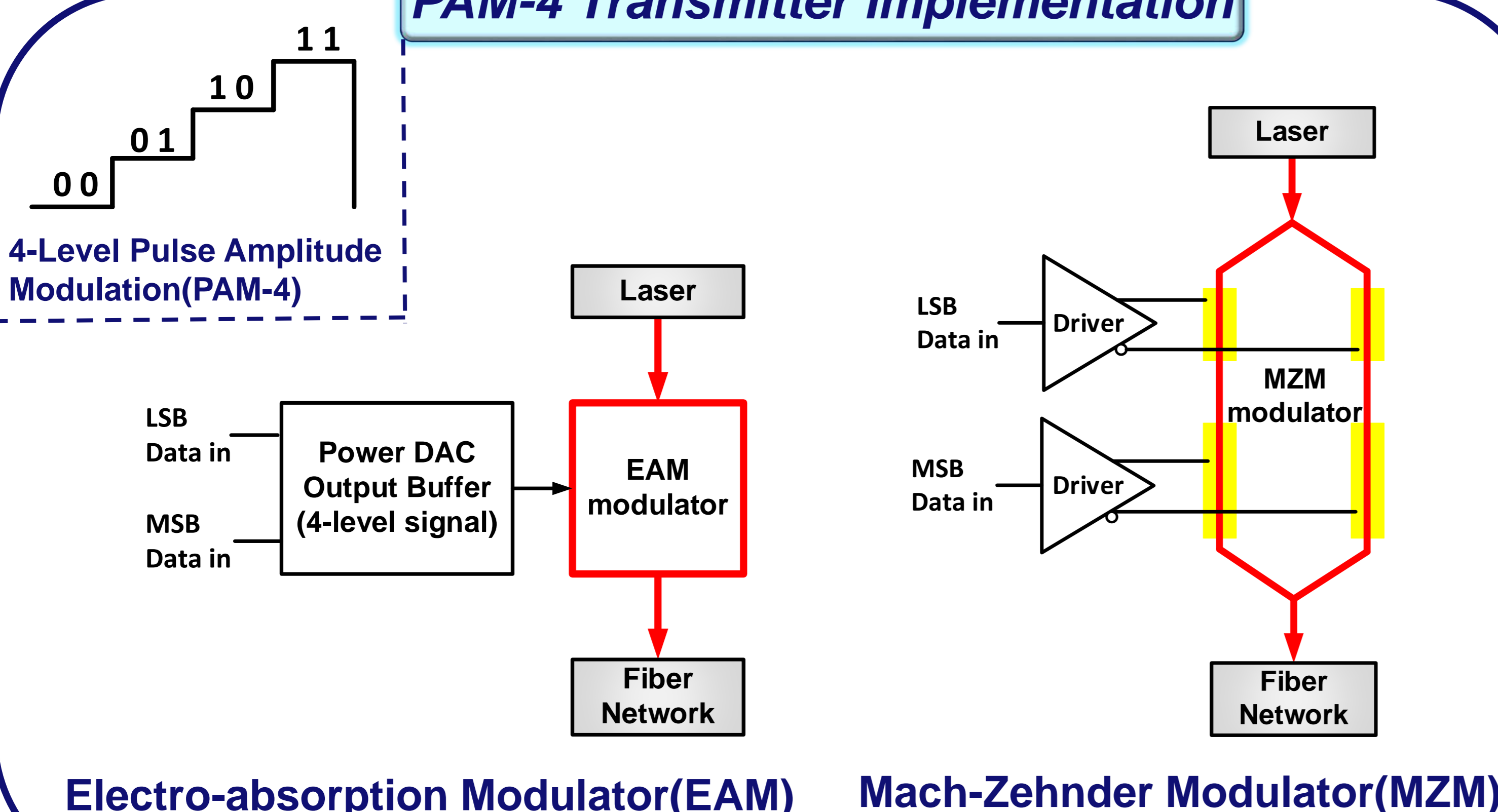
Wafer Alignment



Co-design Challenges

- Floorplan of optical and electronic components
- Simulation and optimization of heating effects on device performance
- Combined optical and millimetre wave measurement setups

PAM-4 Transmitter Implementation



Targets

- Optical transceivers with high data rate beyond 400 Gb/s: 8 channels with 50 Gb/s
- Modulator bandwidth > 25 GHz
- Good heat dissipation design
- High power efficiency

Photonics



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