Hybrid integration of photonics and electronics using wafer scale polymeric bonding techniques

J.J.G.M. van der Tol

Eindhoven University of Technology, P.O. Box 513, 5600 MB Eindhoven, The Netherlands
The real authors.....
Outline

• Introduction
• EU H2020 [WIPE] Project: Wafer-scale Integration of Photonics and Electronics
• Wafer Bonding & Interconnects Technology
• Electronic – Photonic Circuitry Co-Design
• Packaging and Thermal Issues
• Conclusion
Clouds and Distributed Computing

- Huge growth in datacenter network bandwidth requirements
  - Photonics-Enabled Disaggregated Data Centers

- 400G or future Tb/s Ethernet
  - high serial rates for 500m and 2km single-mode fibre applications
  ⇒ lower lane counts, higher spatial efficiency

- Datacenter/HPC: optical interconnects are needed!
  - Low power consumption
  - Low cost solutions

*Amin Vadhat, Google, Interop’16 Keynote*
Philosophy of WIPE

• Use mature electronics
  – BiCMOS-wafers
  – Obtained from foundry
• Use mature photonics
  – Indium phosphide platform
  – Obtained from foundries
• Bringing these together
  – Bonding
  – Co-design of electronic and photonic circuits
  – Develop electrical, optical, thermal connections
  – Dicing and Packaging
• Aim for relevant applications
  – Datacom
  – 400 Gb/s

http://wipe.jeppix.eu/about-us.html
WP1 Objectives

- Exemplifying and benchmarking the key WIPE concepts
- Technological architecture & co-design tool development
Hybrid integrated electronics and photonics on wafer scale → WIPE concept

a (Bi)CMOS-compatible way to attach a photonic layer to an integrated electronic circuit which is generic to many combinations of photonic and electronic wafers.
Horizon 2020 contract number 688572

- **Photonic layer**
  - Adhesion and planarization layers

- **Electronics layers**
  - Dielectric layers and metals

Off-chip connections via the electronic circuits
p-InP
active material
Q1.06 (WG layer)
p- InP
Q1.3/ InGaAs etch stop layer
InP substrate
WIPE Wafer Bonding & Interconnects

Processing devices
Single project wafer run
WIPE Wafer Bonding & Interconnects

Polymer processing
Flip InP
WIPE Wafer Bonding & Interconnects

BiCMOS wafer
Marker backside InP wafer
WIPE Wafer Bonding & Interconnects

Bonding
InP Substrate removal
WIPE Wafer Bonding & Interconnects

Realization of interconnects
Bonding & Interconnects: Initial Results

- Bonding test: top view on the result after substrate & etch stop removal ⇒ no cracks visible

- Interconnects: process realized with multi resist layer deposition and Fluoride-based dry etch ⇒ resistance in the order of 100 mOhm/cm
DFB+ EAM vs EML

- All BB now available
  - DFB (P or Al)
  - EAM (Al)
  - EML (Al)
WIPE EIC Development

Gen. 0

Calibration and Test Structures

Gen. 1

2-channel 56Gb/s PAM-4 EAM driver

2-channel 56Gb/s PAM-4 TIA receiver
Sub-assembly Design: Mechanical

Mechanical scheme and design
• Photronic chip stack attached to the PCB using silver-filled epoxy resin for die bonding
• Heat sinks attached using the same resin or by solder
• Top heat sink only if strictly required

- Photronic chip stack attached to the PCB using silver-filled epoxy resin for die bonding
- Heat sinks attached using the same resin or by solder
- Top heat sink only if strictly required

- PCB for Rx and Tx chip testing
- Rx chip
- Tx chip
- SM fiber
- Adhesive glob to fix fiber to WG facet
- Adhesive glob as stress reliever for fiber
- Cross section of package showing thermal vias in the PCB under the chip
• Include heat spreader (2 µm Au)

➢ Al-based laser should work
➢ P-based laser possible

Thermal Simulations: TX Chip

Front view simulation

Temperature increase of InP with heat spreader
Conclusion

• Effective co-design and co-integration of photonics and electronics allows for miniaturization and subsequently energy and cost savings.

• We describe the EU H2020 WIPE approach towards photonic/electronic integrated circuitry co-design/co-optimization and wafer-scale integration.

• Initial results are promising and the WIPE technologies have potential to enable next-level photonic/electronic integration.
Thank you for your attention

Any Questions?

Check out our blogs on LinkedIn:
https://www.linkedin.com/company/wipe-photronics/