Background of the WIPE project

In our current information society we generate and store huge amounts of data, for which we increasingly use computer servers in large data centers. All these servers and data centers jointly form an enormous data repository (also called 'the cloud') in which both companies and consumers can store their data. This cloud data storage facility enables us to watch video at any time we like (video-on-demand services like Netflix), listen to the music we want to hear (using streaming services like Spotify) and store our photos and documents. Consumers are most probably familiar with cloud services like Google Drive and Google Photo, Apple iCloud, Microsoft OneDrive, Dropbox, etc. An impression of how a data center looks like from the inside is given in *Figure 1*.

Figure 1: Rows of cabinets full of computer servers in a data center.

To access and exchange these data in a reasonable time, we need very high speed data communication connections. Currently, much of the internet data network in between data centers is formed by optical fibres which allow the exchange of information at a tremendously high speed using light (photons) running through very thin fibreglass wires. The data network between the computer servers inside data centres must be extremely fast as well since they cooperate and exchange data too. Currently, fiber optical interconnection solutions are available (*Figure 2*), but a demand exists for ever higher data exchange rates. Ultrafast interconnects of 400 Gigabits/second and larger are asked for. Using today's technology, these interconnections require complex and expensive electronic-photonic components which consume much energy and take up much space.

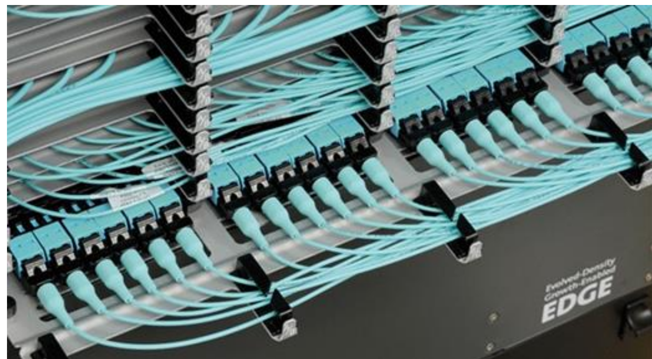

Figure 2: Data interconnect cables for exchange of data between computer servers in a data center.

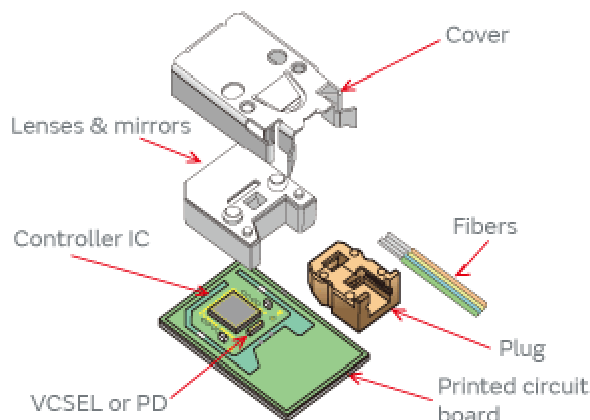

Figure 3: Interior of a high speed connector holding an electronic-photonic signal transceiver

The connector in which electronic signals are transformed to optical signals generally require both a light emitting (photonic) integrated circuit (PIC) and an electronic chip (IC). The ICs contain the driver, receiver and control electronics for the PIC. The PIC generates the photonic signals (i.e. light) and is connected to an optical fibre. In current high speed connectors, the PIC and IC are mounted together on a printed circuit board and connected to each other using wire bonds as shown in figure 3. This is a costly solution since the connector contains several components which need to be assembled. Moreover, the long wire bond connections limit the communication speed between IC and PIC, and thus of the entire connector. So the wired connections between PIC and IC must be as short as possible.

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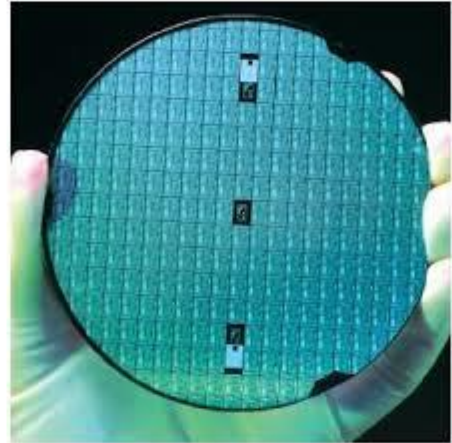
Objectives of the WIPE project

Photonic and electronic IC connection technology development

The WIPE project aims at developing a technology to solve the problem of the speed limitation by connecting the electronic (ICs) and photonic chips (PICs) very intimately, placing them on top of each other, thus eliminating the need for bond wires. To reduce the cost of this approach, it is the aim to connect ICs and PICs when they are still embedded on the production 'wafer' of semi-conductor material, see figure 4. For this reason, the project is called 'Wafer scale Integration of Photonics and Electronics (WIPE)'. This 'wafer scale integration' technology enables the creation of high performance and high density photonic-electronic (sometimes called 'photronic') modules, having higher data transmission rates at lower energy consumption, lower complexity and lower cost compared to modules using more traditional connection techniques of the separate chips shown in *figure 3*. An impression of the intimately connected photronic device is given in *Figure 5*.

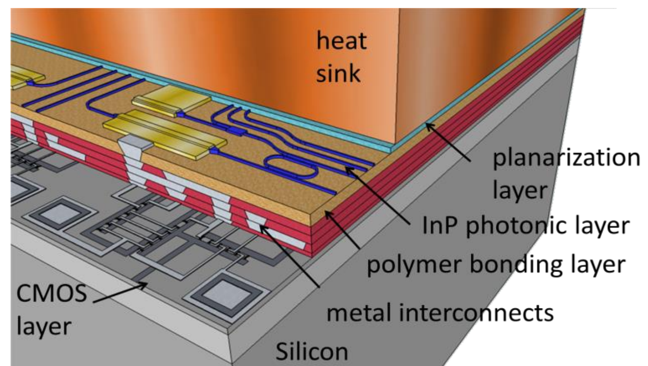
Figure 4: An example of a wafer containing integrated circuits. These can be electronic or photonic circuits. For each type, a different semiconductor material is needed. Silicon is used for the electronic ICs, the photonic ICs are made of Indium Phosphide.



Development of electronic-photonic co-design tools

Next to the novel bonding technology of ICs and PICs, an integrated module development methodology is created for the efficient co-design of ICs and PICs which need to fit exactly onto each other, both physically, electronically and thermally. A library consisting of photonic/electronic standard design elements is created, leveraging the process design kits (PDKs) of the most important European manufacturers of photonic chips with that of a powerful IC-manufacturer. These tools are of significant importance to the industry, since they offer photronic module designers a standardised approach that highly facilitates the module design abilities of SMEs and affordable manufacturing by the photonic and electronic foundries. The PDK is demonstrated by prototyping a 400Gb/s transceiver for data center applications as mentioned earlier. In doing so, the WIPE project aims at bringing photonics to a new level by developing a concept that can be well industrialised..

Figure 5: Artist's impression of a cross-section for an integrated photonic/electronic chip, showing the silicon electronics CMOS layer and the InP photonic layer, with the metal interconnect stack and the polymer bonding layer in between, and heat sink on top. The optical coupling and bottom of the chip-stack are not shown.



Activities within the WIPE project

The project has been divided into three main design stages:

0. The experimentation phase of joining the ICs and PICs ('sticking' them on top of each other) with great alignment accuracy and making the electrical connections. In this phase the joining

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and connection process is studied and optimized, while the properties of the connected chips, esp. the properties of the electronic interconnects and the connection of the PIC to the optical fiber, are studied and characterized. These properties must be known in order to make a proper electronic-photonic design of the assembled unit.

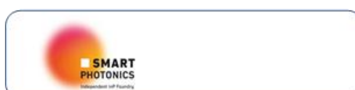
1. The development of a one-channel (50 Gbit/s) transceiver device as proof of concept for the technology. The IC and PIC need to be co-designed for proper functioning when connected. Electronical, optical, thermal and mechanical properties of the chips must be considered carefully in view of the very different properties when mounted on top of each other. Additional process development is conducted.
2. The demonstration of an eight-channel device (400 Gbit/s) providing the final prototype of the technology.

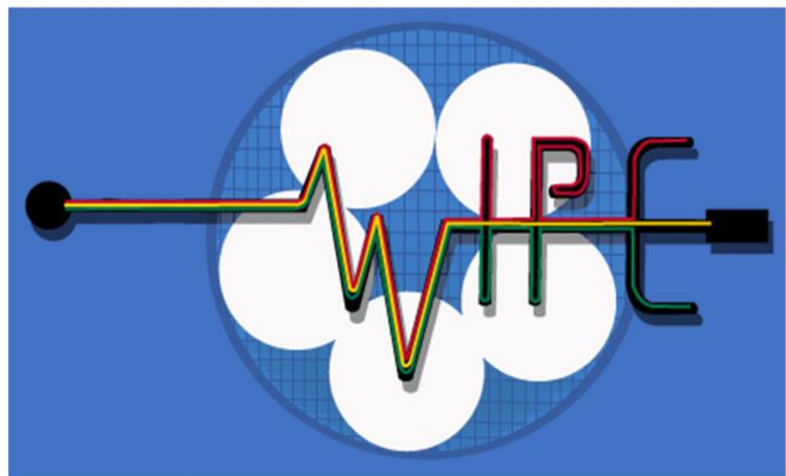
WIPE project progress

At half time, process research of stage-0 is still in progress while the IC and PIC designs for the stage-1 single channel prototype are nearly completed.

The technology development is concentrating on the following challenges:

- a technique for accurately aligning the InP and silicon wafers in order to stack them with a tolerance of less than 2 micrometer,
- experiments to establish a proper fixation and curing process for the polymer wafer bonding layer that does not introduce too much mechanical stress,
- development of etching and metal deposition techniques to manufacture the high frequency electrical interconnect between the photonic and electronic chips,
- creating a low loss optical coupler to the outside world (fiber) on the photonic chip,
- mapping the heat generation during operation in the photronic chip stack and finding ways to drain this heat to the outside world as a part of the photronic device packaging.





Wafer scale Integration of Photonics and Electronics

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